

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	APPD DATE
			2011-04-08

K78 MLB SCHEMATIC

04/08/11

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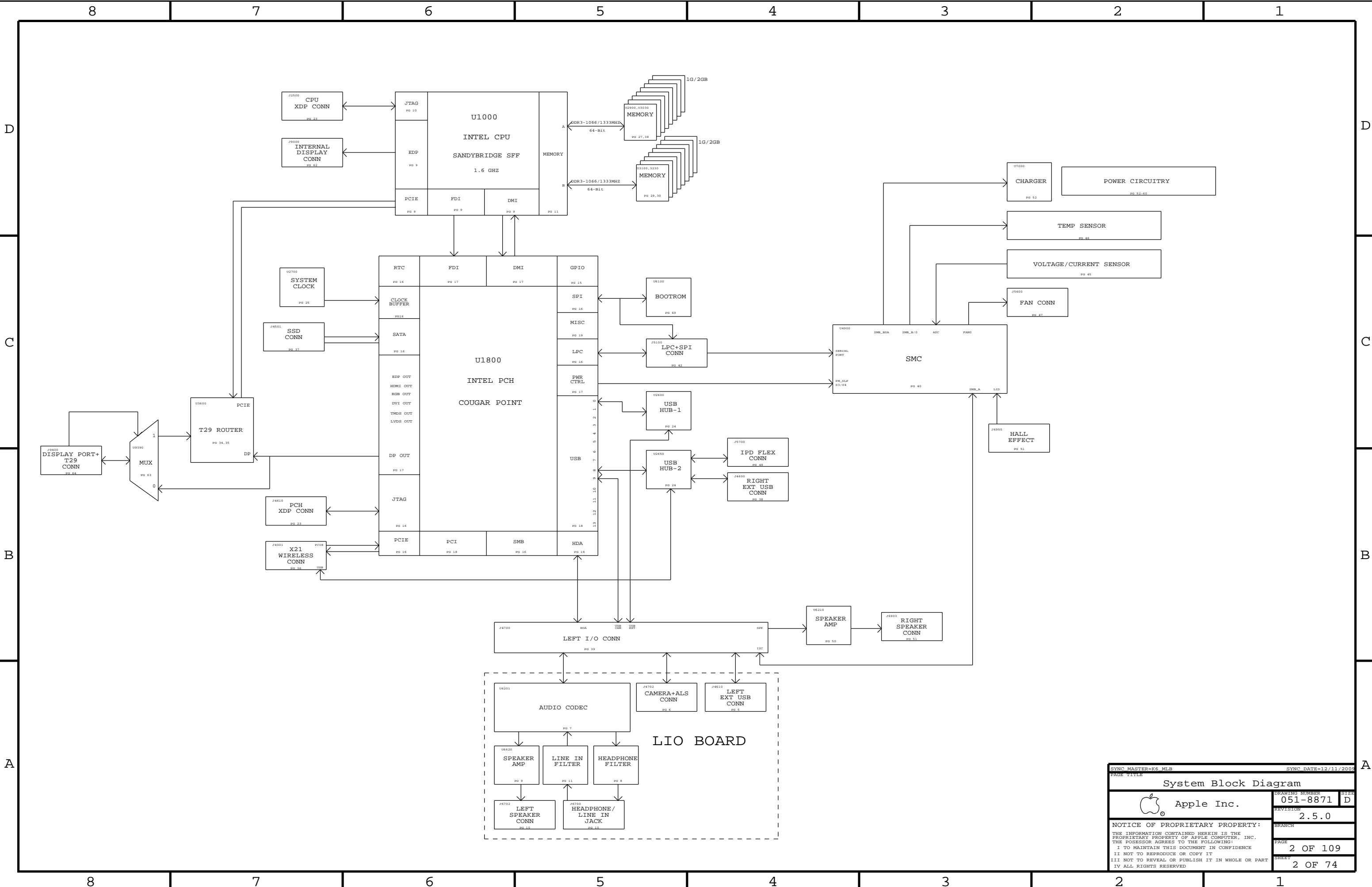
Schematic / PCB #'s

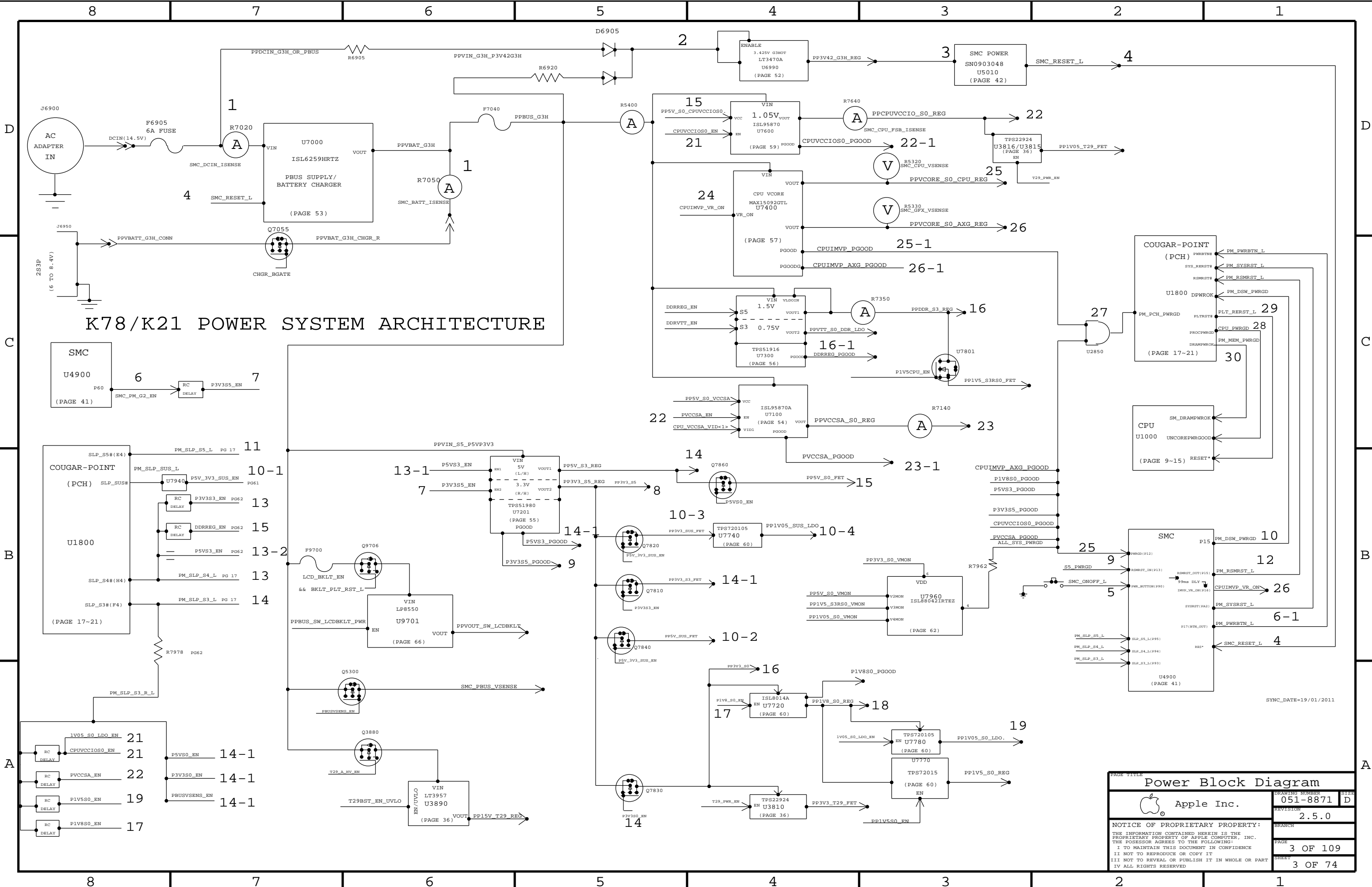
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8871	1	SCHEN,MLB,K78	SCH	CRITICAL	
820-3024	1	PCBP,MLB,K78	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Fri Apr 8 10:21:51 2011

PRODUCT SAFETY REQUIREMENTS:
PCB, UL RECOGNIZED, MIN. 130-C TEMP. RATING AND V-0 FLAME RATING PER UL 796 & UL 94.
PCB TO BE SILK-SCREENED WITH UL/CUL RECOGNITION MARK, MANUFACTURER'S UL FILE
NUMBER, UL PCB MATERIAL DESIGNATION, 130-C TEMP. RATING AND V-0 FLAME RATING.


DRAWING TITLE		SCHEM, MLB, K78	
 Apple Inc.	DRAWING NUMBER		SIZE
	051-8871		D
	REVISION		
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K78/K21 POWER SYSTEM ARCHITECTURE

Power Block Diagram

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SYNC_DATE=19/01/2011

[illegible]

K78 BOM GROUPS

BOM GROUP	BOM OPTIONS
K78_COMMON	ALTERNATE,COMMON,K78_MISC,K78_DEBUG:ENG,K78_PROGPARTS,USBHUB_2513B,T29BST:Y,EDP
K78_MISC	PCH:B3,CPUMEM_S0,HUB1_2NONREM,HUB2_2NONREM,T29:YES,SDRVI2C:MCU,SDRV_PD,KB_BL
K78_PROGPARTS	BOOTROM_PROG,SMC_PROG,T29ROM:PROG,T29MCU:PROG
K78_DEVEL:ENG	BLKT:ENG,BMON:ENG,XDP_CONN,XDP_CPU:BPW,XDP_PCH,LPCPLUS,VREFMGRN,SGPOOD,ISL,S3_S0_LED,VCCIOISNS_ENG,AIRPORTISNS_ENG,REDISNS_ENG,LCDDBKLTISNS_PROD
K78_DEVEL:PVT	LPCPLUS,XDP_CONN,XDP_PCH
K78_DEBUG:ENG	DEVEL_BOM,SMC_DEBUG_YES,XDP
K78_DEBUG:PVT	DEVEL_BOM,BLKT:PROD,BMON:PROD,SMC_DEBUG_YES,XDP,VREFMGRN_NOT
K78_DEBUG:PROD	BLKT:PROD,BMON:PROD,SMC_DEBUG_YES,XDP,VREFMGRN_NOT,LPCPLUS,VCCIOISNS_PROD,AIRPORTISNS_PROD,HDDISNS_PROD,LCDDBKLTISNS_PROD
DDR3:HYNIX_2GB	DRAM_CFG0:L,DRAM_CFG1:L,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:HYNIX_2GB
DDR3:HYNIX_4GB	DRAM_CFG0:L,DRAM_CFG1:L,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:HYNIX_4GB
DDR3:SAMSUNG_2GB	DRAM_CFG0:L,DRAM_CFG1:H,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:SAMSUNG_2GB
DDR3:SAMSUNG_4GB	DRAM_CFG0:L,DRAM_CFG1:H,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:SAMSUNG_4GB
DDR3:MICRON_2GB	DRAM_CFG0:H,DRAM_CFG1:L,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:MICRON_2GB
DDR3:ELPIDA_4GB	DRAM_CFG0:H,DRAM_CFG1:H,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:ELPIDA_4GB

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
33580550	1	EEPROM,32KBIT,2X10PH	U3690	CRITICAL	T29ROM:BLANK
34170354	1	IC,T29-BOM,K78	U3690	CRITICAL	T29ROM:PROG
33783997	1	IC,MCU,32B,LPC1112A,168B/35B,HYQFN325	U9330	CRITICAL	T29MCU:BLANK
34170355	1	IC,T29-MCU,K78	U9330	CRITICAL	T29MCU:PROG
33880895	1	IC,SMC,RENESAS,H8B/2117SP,99K,TLP,HP	U4900	CRITICAL	SMC:BLANK
34170350	1	IC,SMC,K78	U4900	CRITICAL	SMC:PROG
33580809	1	64 MBIT SPI SERIAL DUAL 1/O FLASH,WEIRD: 6	U6100	CRITICAL	BOOTROM:BLANK
33580803	1	64 MBIT SPI SERIAL DUAL 1/O FLASH,WEIRD: 8	U6100	CRITICAL	BOOTROM:BLANK
34170349	1	IC,RF1 ROM,K21 K78	U6100	CRITICAL	BOOTROM:PROG

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
37680855	37680613		ALL	Diodes alt to Toshiba
37680977	37680859		ALL	Diodes alt to Toshiba
37680972	37680612		ALL	RoHS alt to Toshiba
37700107	37700566		ALL	Onsemi alt to Semtech
13880676	13880691		ALL	Murata alt to Samsung
37180679	37180652		ALL	NXP alt to NXP
13880671	13880673		ALL	Taiyo alt to Murata
13880678	13880678		ALL	Murata/Samsung alt to Taiyo
35303312	35303055		ALL	NXP ALT TO PERICOM
10400035	10400011		ALL	Panasonic alt to Cytect
15201086	15201307		ALL	Toko alt to Cytect
15201462	15201295		ALL	Toko alt to NEC Inductor
12803033	12803294		ALL	Sanyo alt to Sanyo/Frederick
33784092	33784100		ALL	EARLY 1.50HZ CPU SAMPLES
33784093	33784101		ALL	EARLY 1.40HZ CPU SAMPLES
37680874	37680895		ALL	FDMC0202 alt to RJX03000S
37681018	37680617		ALL	FDMC0349 alt to RJX0305DB
37680826	37680917		ALL	RJX03320DB alt to FDMG0355
514-0744	998-3941		ALL	mDP connector alt

DRAM CFG CHART


	VENDOR	CFG 1	CFG 0
	HYNIX	0	0
	SAMSUNG	1	0
	MICRON	0	1
	ELPIDA	1	1

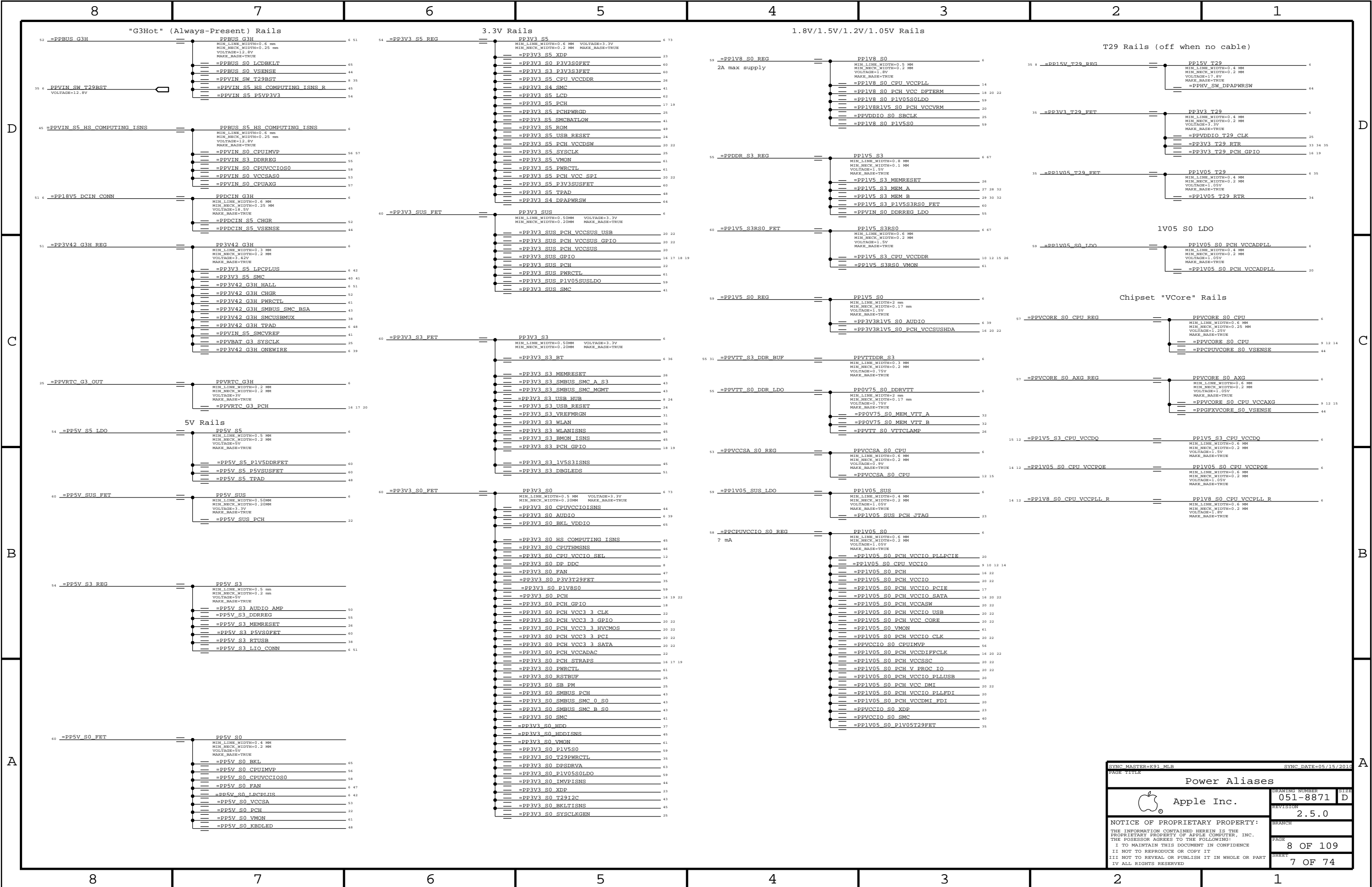
SIZE	CFG 2
2GB	0
4GB	1

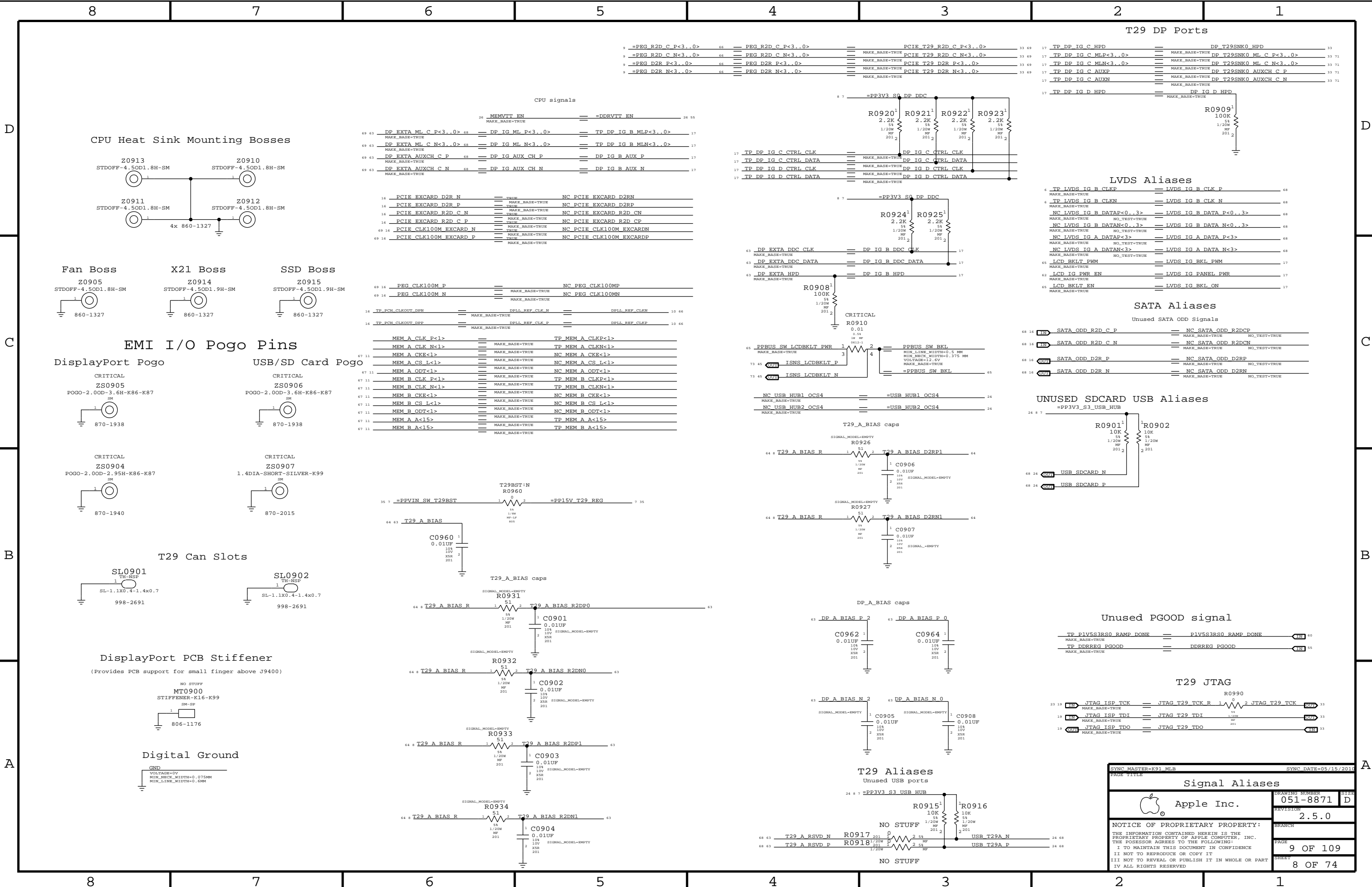
Module Parts


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4101	1	SNB_QAM1,Q5,J1,1.6,17W,2+2,1.1,4M,BGA	U1000	CRITICAL	CPU:1.6GHZ
337S4100	1	SNB_QAM2,Q5,J1,1.5,17W,2+2,1.1,4M,BGA	U1000	CRITICAL	CPU:1.5GHZ
337S4099	1	SNB_QAM3,Q5,J1,1.4,17W,2+2,1.05,3M,BGA	U1000	CRITICAL	CPU:1.4GHZ
337S4098	1	SNB_QALV,Q5,J1,1.3,17W,2+2,1.05,3M,BGA	U1000	CRITICAL	CPU:1.3GHZ
337S4080	1	COUGAR_POINT,SLM4G,PRQ,RD82Q567	U1800	CRITICAL	PCB:B2
337S4091	1	COUGAR_POINT,B3,SL4K,PRQ,RD82Q567	U1800	CRITICAL	PCB:B3
338S0976	1	IC,T29,FCBGA,PRQ 8x9MM	U3600	CRITICAL	T29:YES

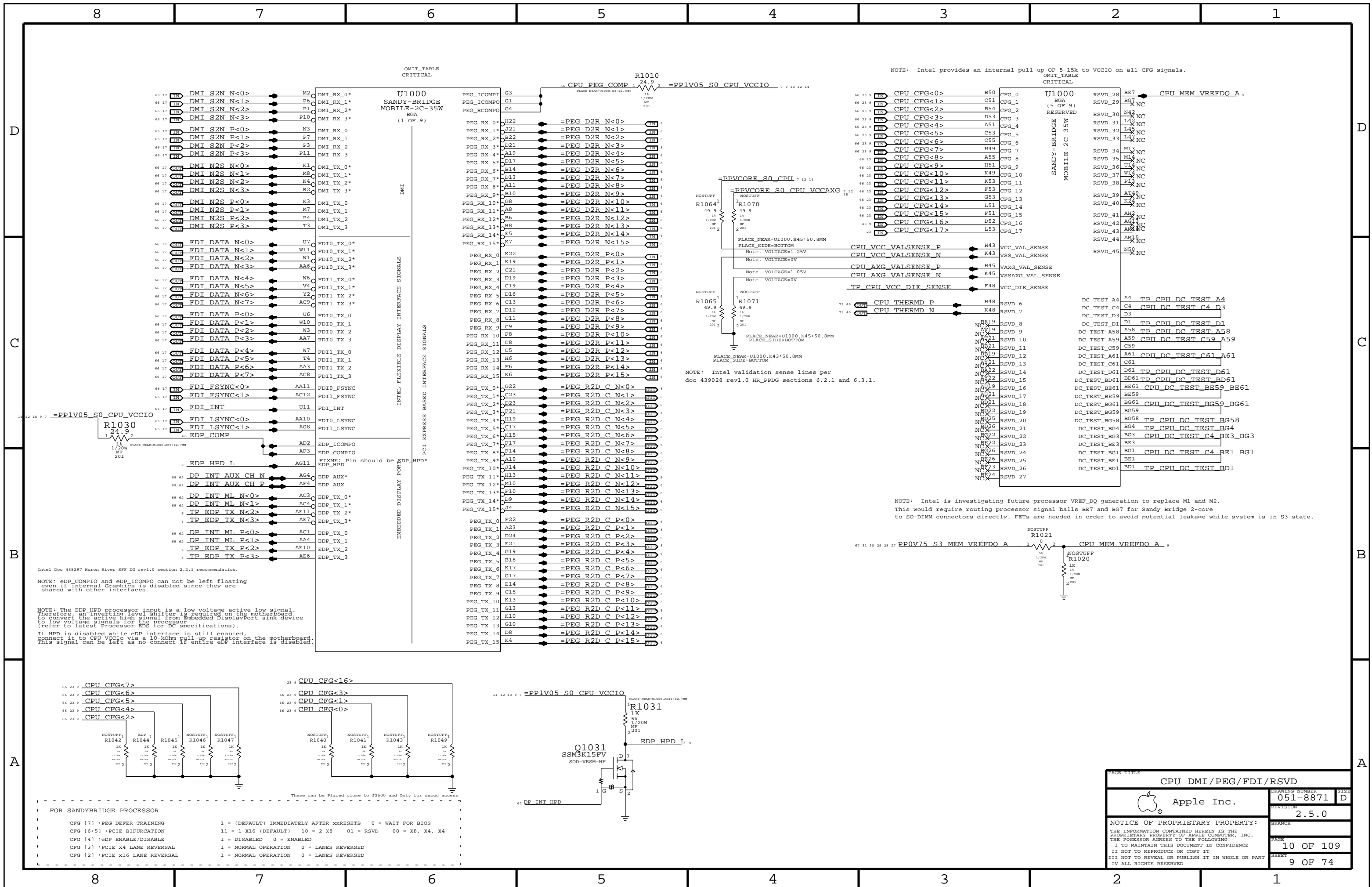
333S0585	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,T-DIE,HYXIX	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE=HYNIX_2GB
333S0585	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,T-DIE,HYXIX	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE=HYNIX_2GB
333S0585	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,T-DIE,HYXIX	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE=HYNIX_2GB
333S0585	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,T-DIE,HYXIX	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE=HYNIX_2GB
333S0586	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,B-DIE,HYXIX	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE=HYNIX_4GB
333S0586	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,B-DIE,HYXIX	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE=HYNIX_4GB
333S0586	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,B-DIE,HYXIX	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE=HYNIX_4GB
333S0586	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,B-DIE,HYXIX	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE=HYNIX_4GB
333S0587	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,G-DIE,SAMSUNG	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE=SAMSUNG_2GB
333S0587	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,G-DIE,SAMSUNG	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE=SAMSUNG_2GB
333S0587	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,G-DIE,SAMSUNG	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE=SAMSUNG_2GB
333S0587	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,G-DIE,SAMSUNG	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE=SAMSUNG_2GB
333S0588	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,D-DIE,SAMSUNG	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE=SAMSUNG_4GB
333S0588	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,D-DIE,SAMSUNG	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE=SAMSUNG_4GB
333S0588	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,D-DIE,SAMSUNG	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE=SAMSUNG_4GB
333S0588	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,D-DIE,SAMSUNG	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE=SAMSUNG_4GB
333S0590	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,V68A-D,MICRON	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE=MICRON_2GB
333S0590	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,V68A-D,MICRON	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE=MICRON_2GB
333S0590	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,V68A-D,MICRON	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE=MICRON_2GB
333S0590	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,V68A-D,MICRON	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE=MICRON_2GB
333S0589	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,C-DIE,ELPIDA	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE=ELPIDA_4GB
333S0589	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,C-DIE,ELPIDA	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE=ELPIDA_4GB
333S0589	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,C-DIE,ELPIDA	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE=ELPIDA_4GB
333S0589	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,C-DIE,ELPIDA	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE=ELPIDA_4GB
607-6811	1	ASSEMBLY,SUBASSY,PCBA,HALL EFFECT,K99	J6955	CRITICAL	
353S2929	1	IC,ISL4259,BATCHCHARGER,31,4C4MM,QFN28	U7000	CRITICAL	

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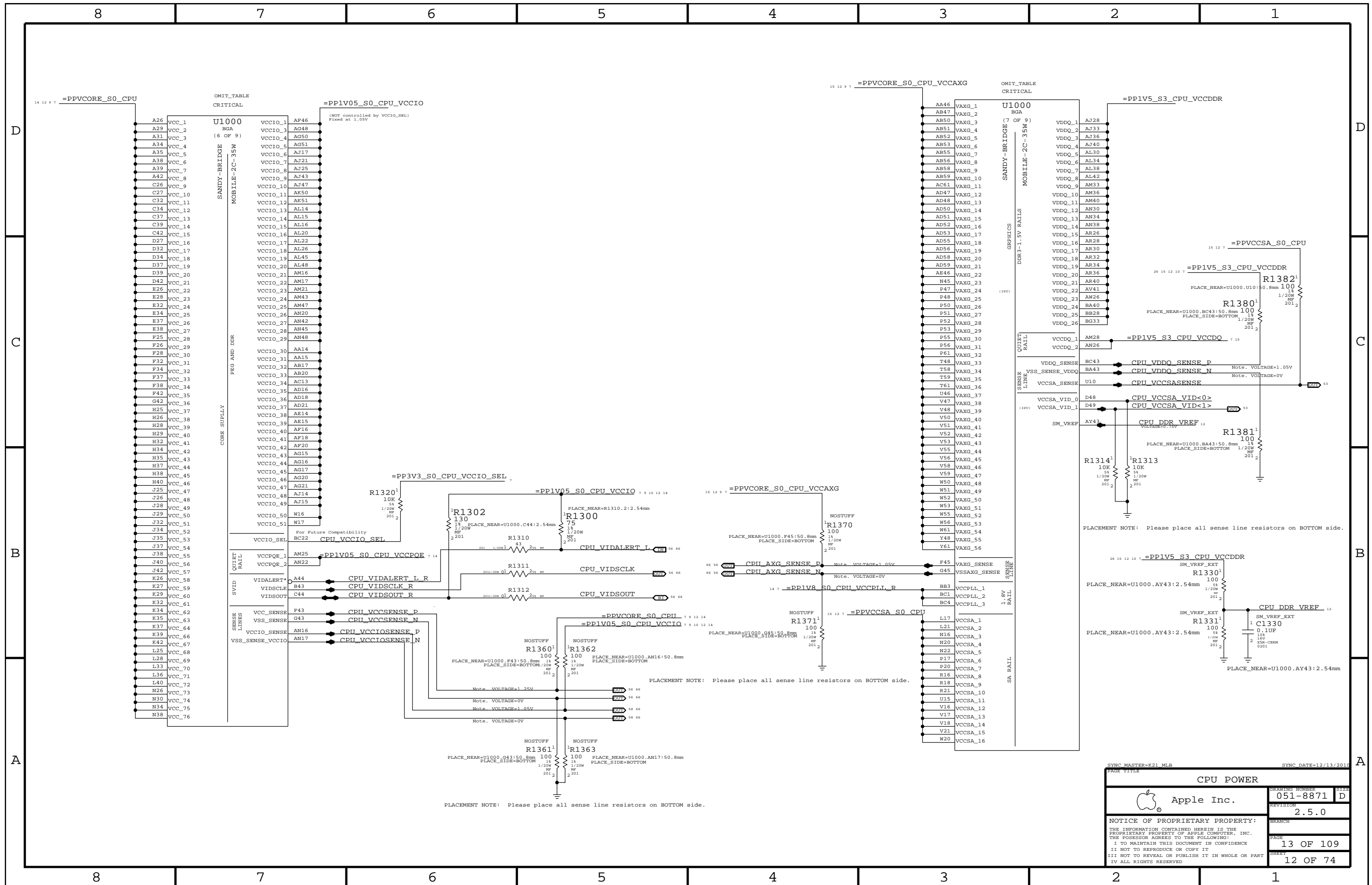


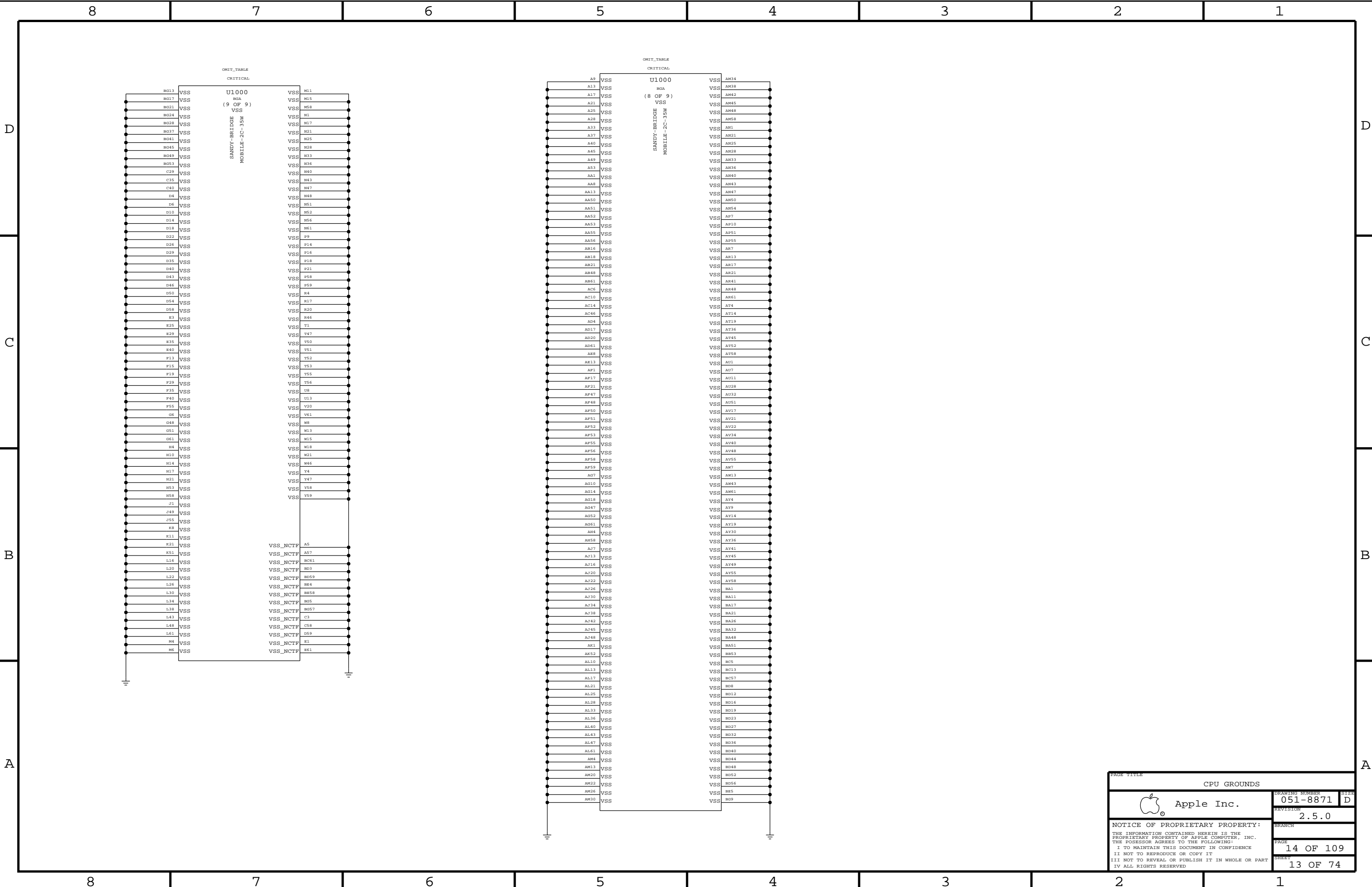


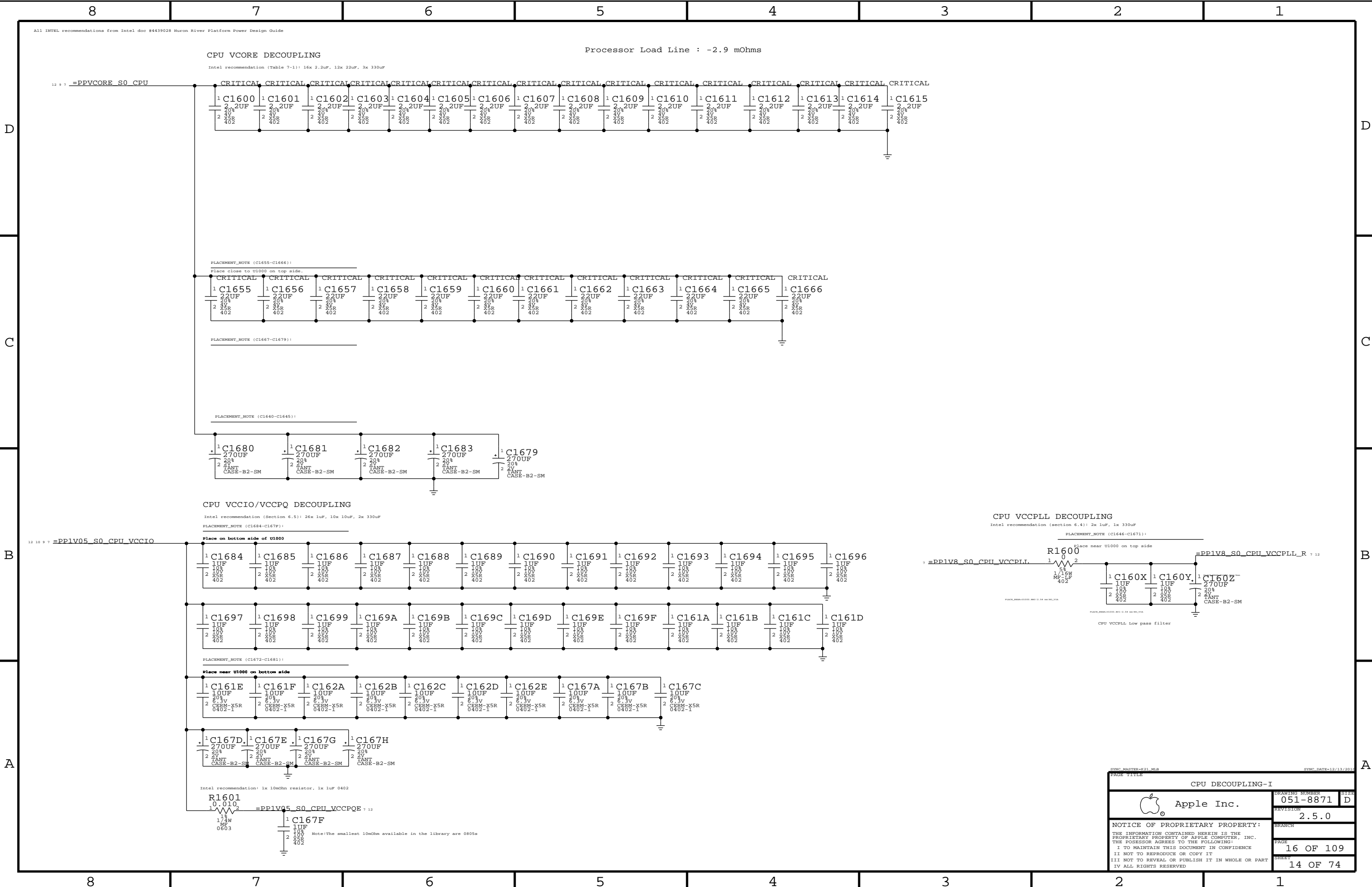
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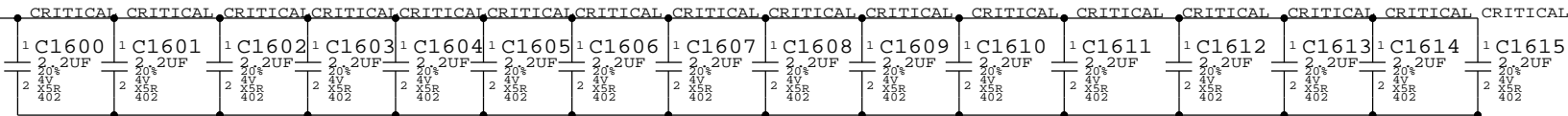




CPU Vcore DECOUPLING

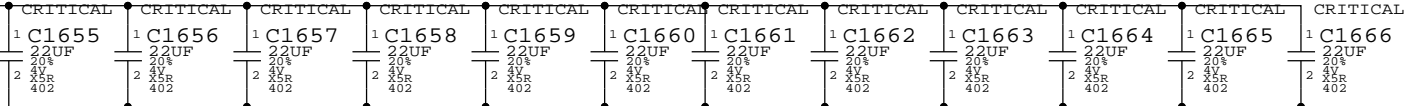
Processor Load Line : -2.9 mOhms

Intel recommendation (Table 7-1): 16x 2.2uF, 12x 22uF, 3x 330uF



PLACEMENT_NOTE (C1655-C1666):

Place close to U1000 on top side.



PLACEMENT_NOTE (C1667-C1679):

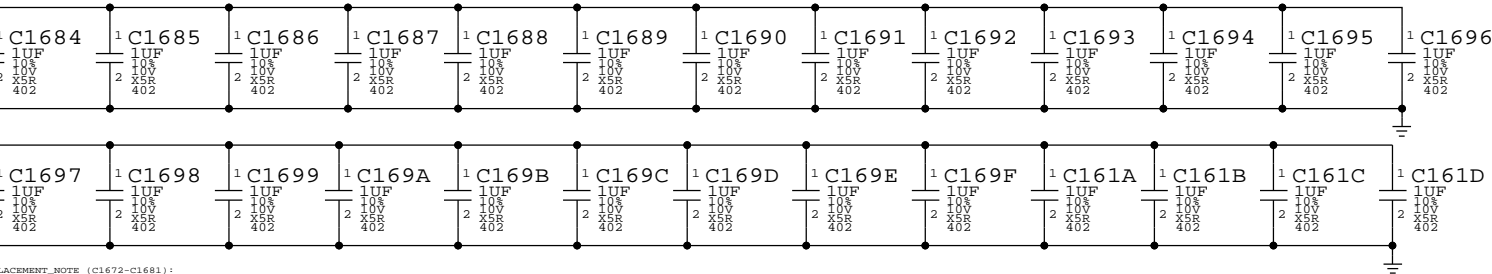
PLACEMENT_NOTE (C1640-C1645):

CPU VCCIO/VCCPQ DECOUPLING

Intel recommendation (Section 6.5): 26x 1uF, 10x 10uF, 2x 330uF

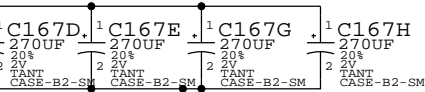
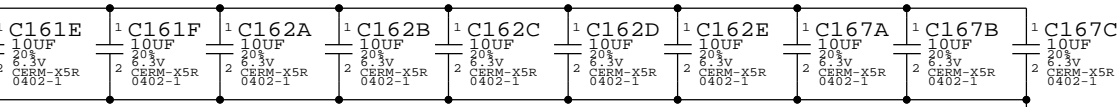
PLACEMENT_NOTE (C1684-C1679):

Place on bottom side of U1000

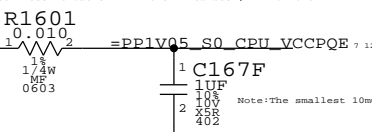


PLACEMENT_NOTE (C1672-C1681):

Place near U1000 on bottom side



Intel recommendation: 1x 10mOhm resistor, 1x 1uF 0402



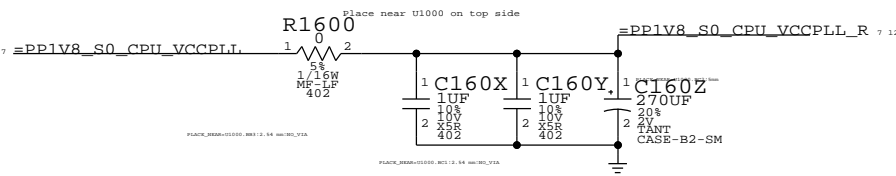
Note: The smallest 10mOhm available in the library are 0805s

CPU VCCPLL DECOUPLING

Intel recommendation (section 6.4): 2x 1uF, 1x 330uF

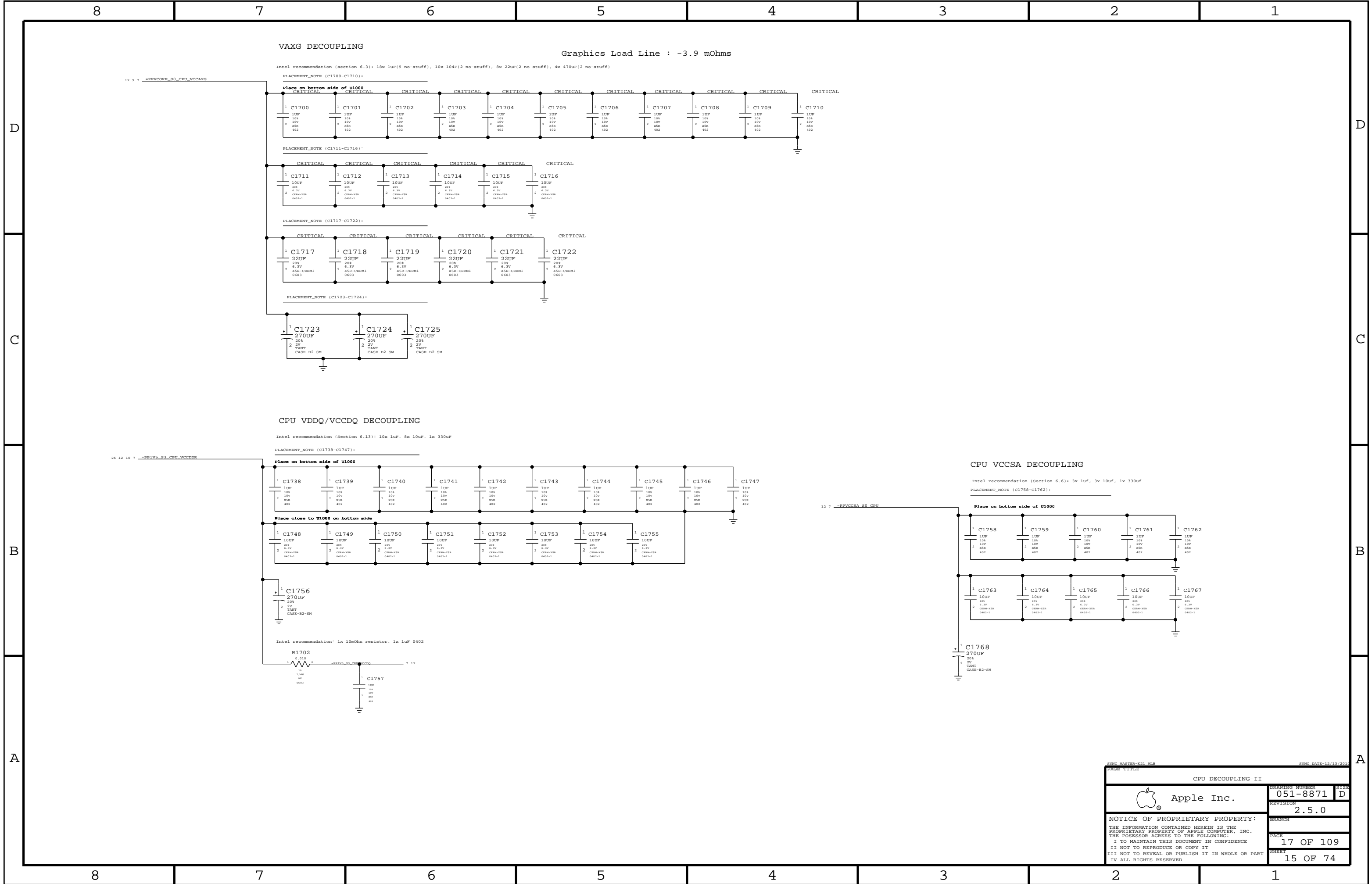
PLACEMENT_NOTE (C1646-C1671):

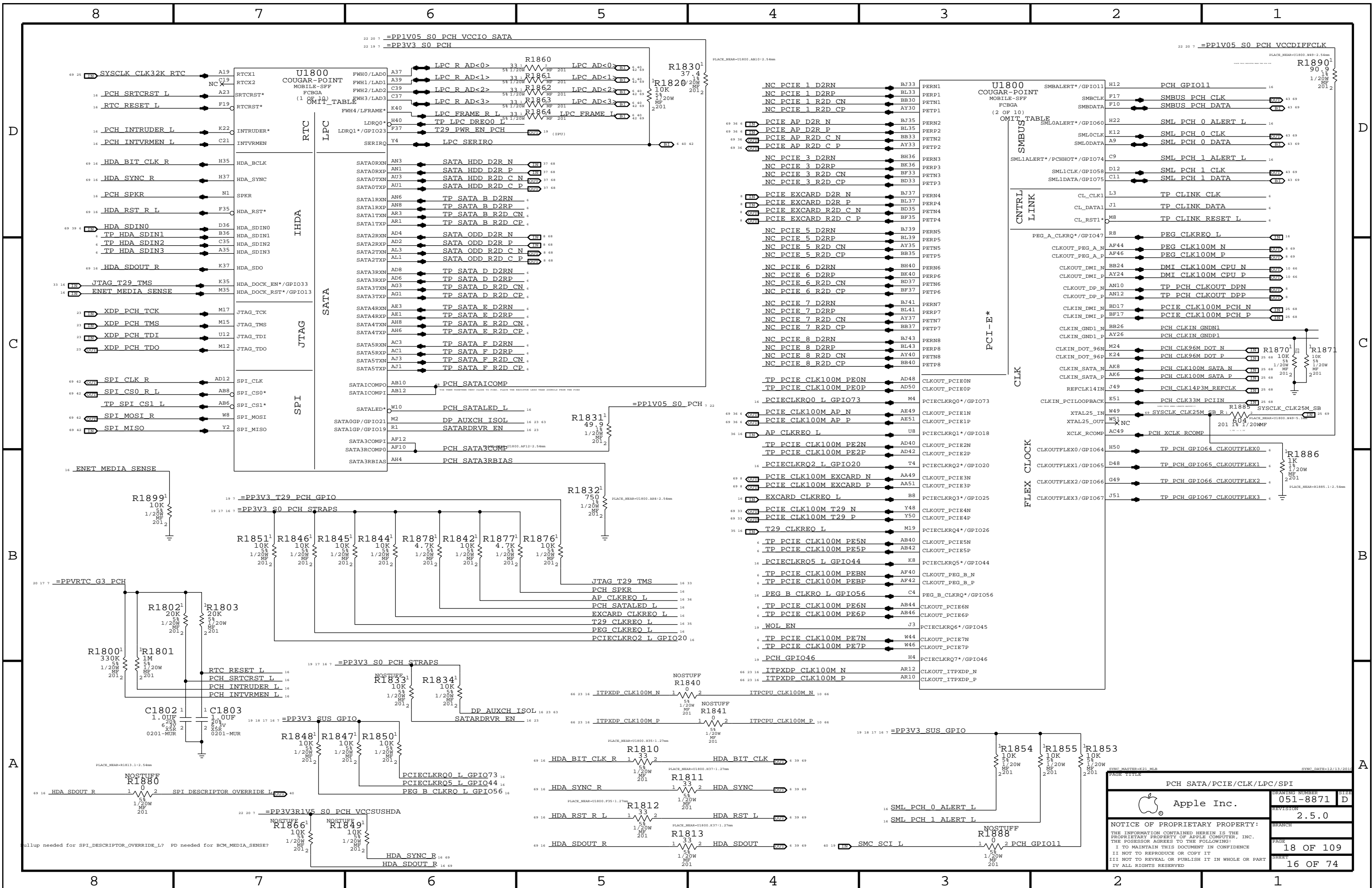
Place near U1000 on top side

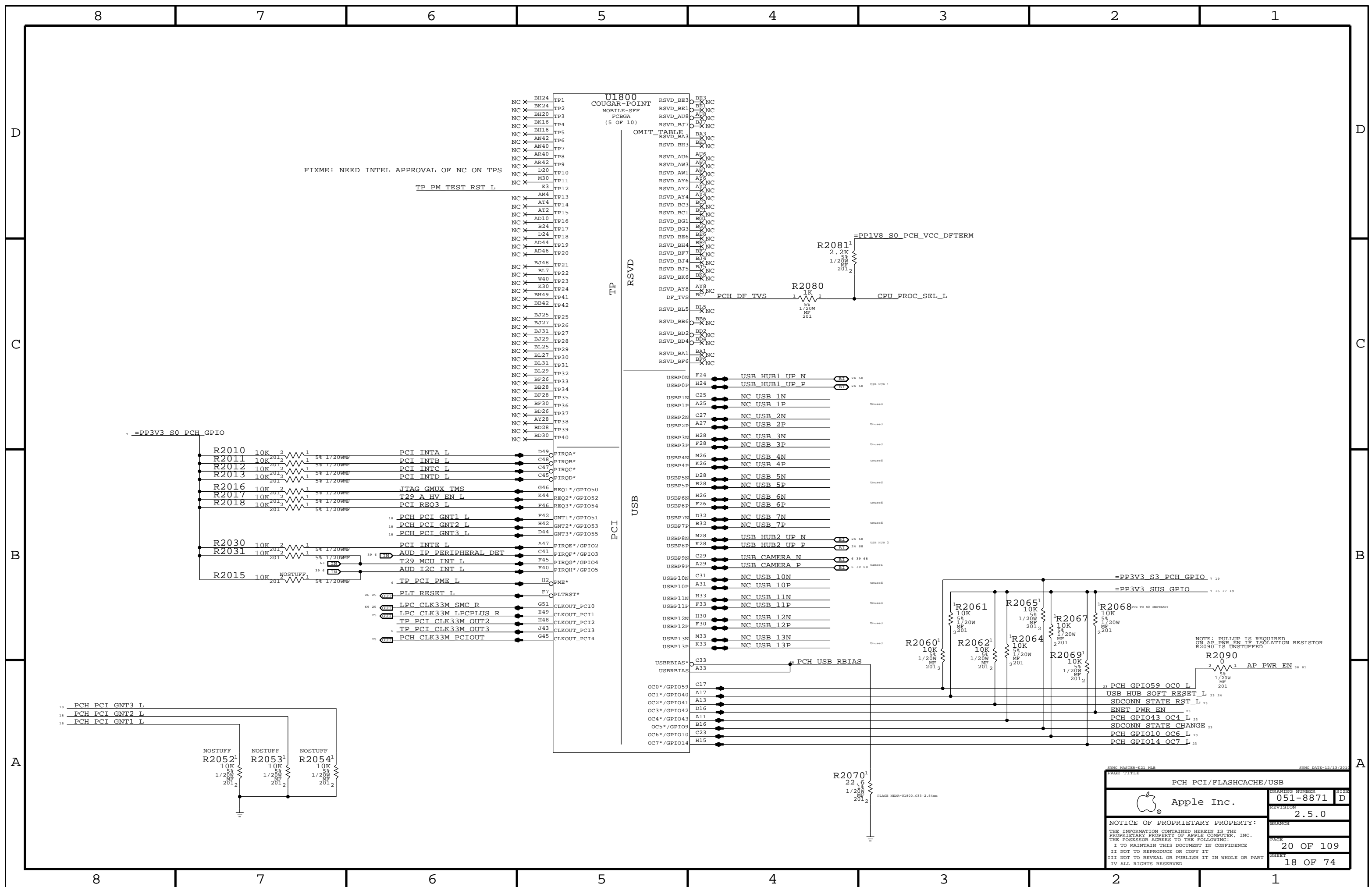


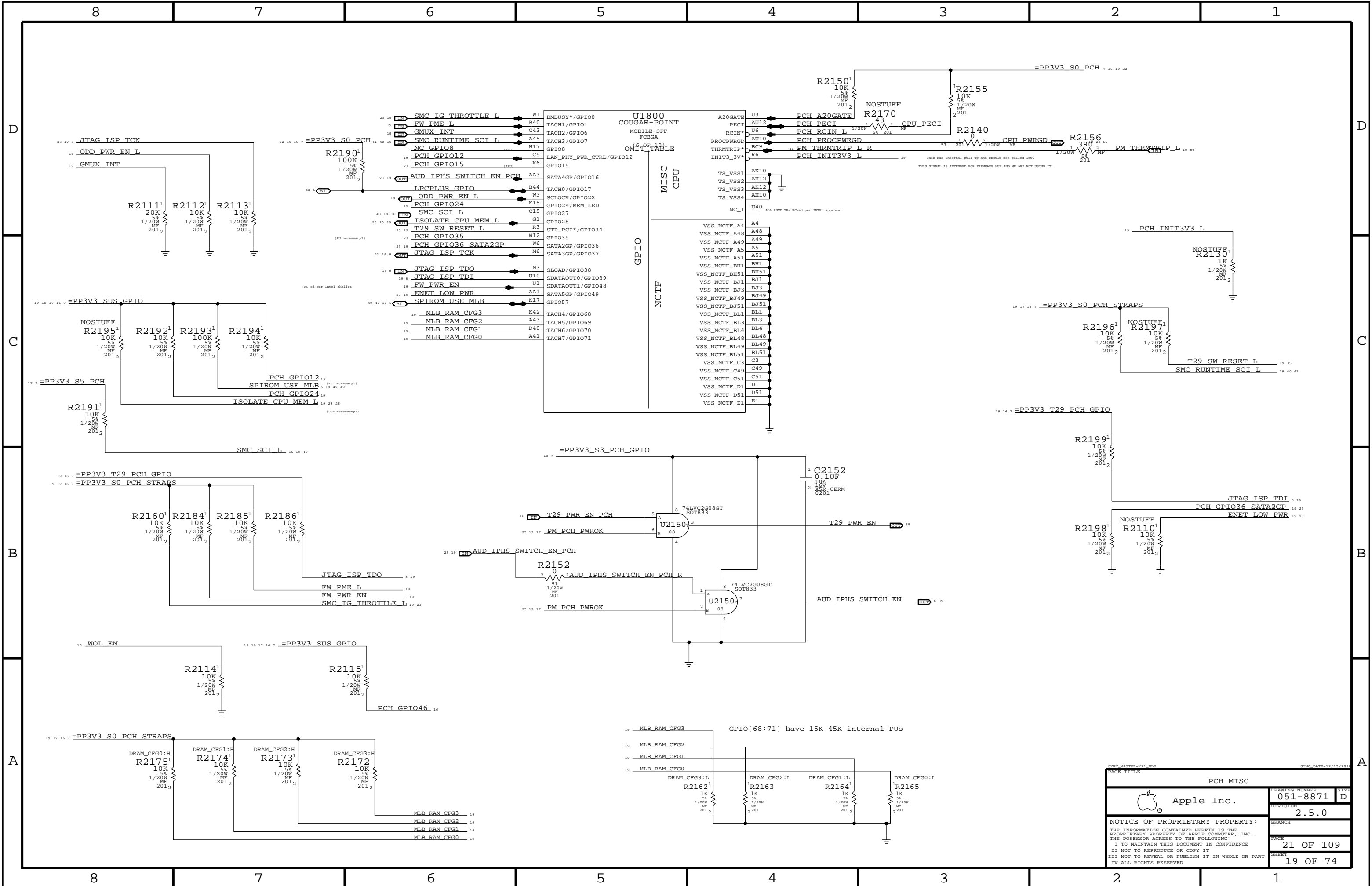
CPU VCCPLL Low pass filter

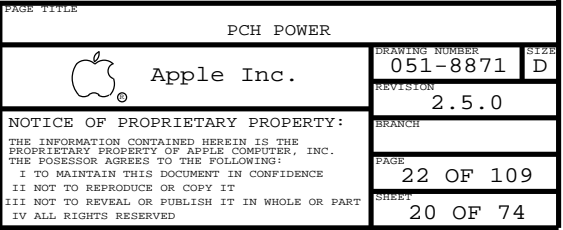
CPU DECOUPLING-I		
Apple Inc.	DRAWING NUMBER	051-8871
	REVISION	2.5.0
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	PAGE	16 OF 109
	SHEET	14 OF 74

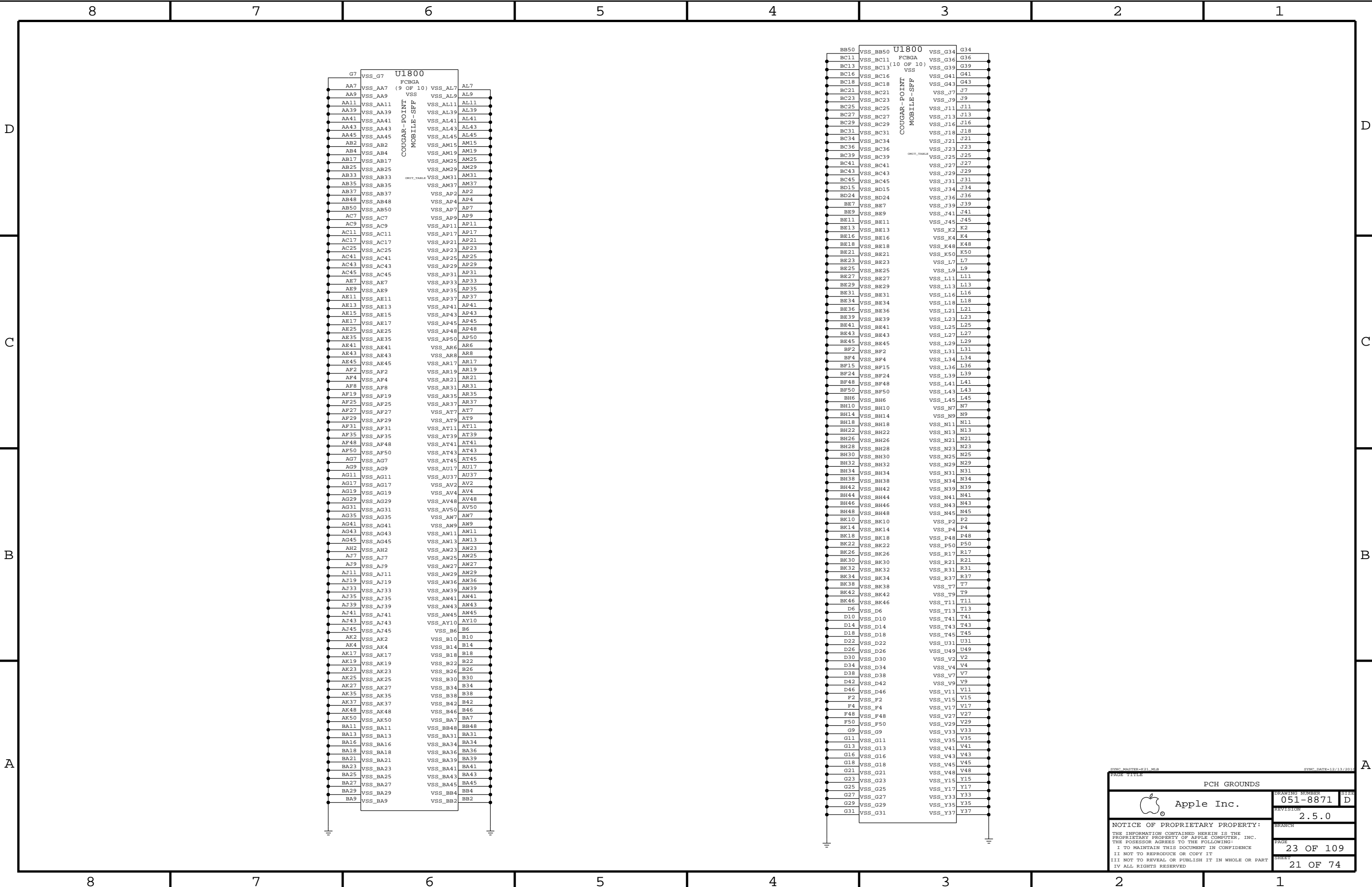




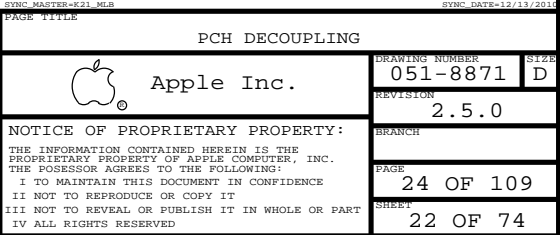








PAGE TITLE		PCH GROUNDS	
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		REVISION	2.5.0
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PROCESSOR MICRO2-XDP CONNECTOR

NOTE: This is not the standard XDP pinout

Use with 920-0782 Adapter Flex to support chipset debug

D

C

B

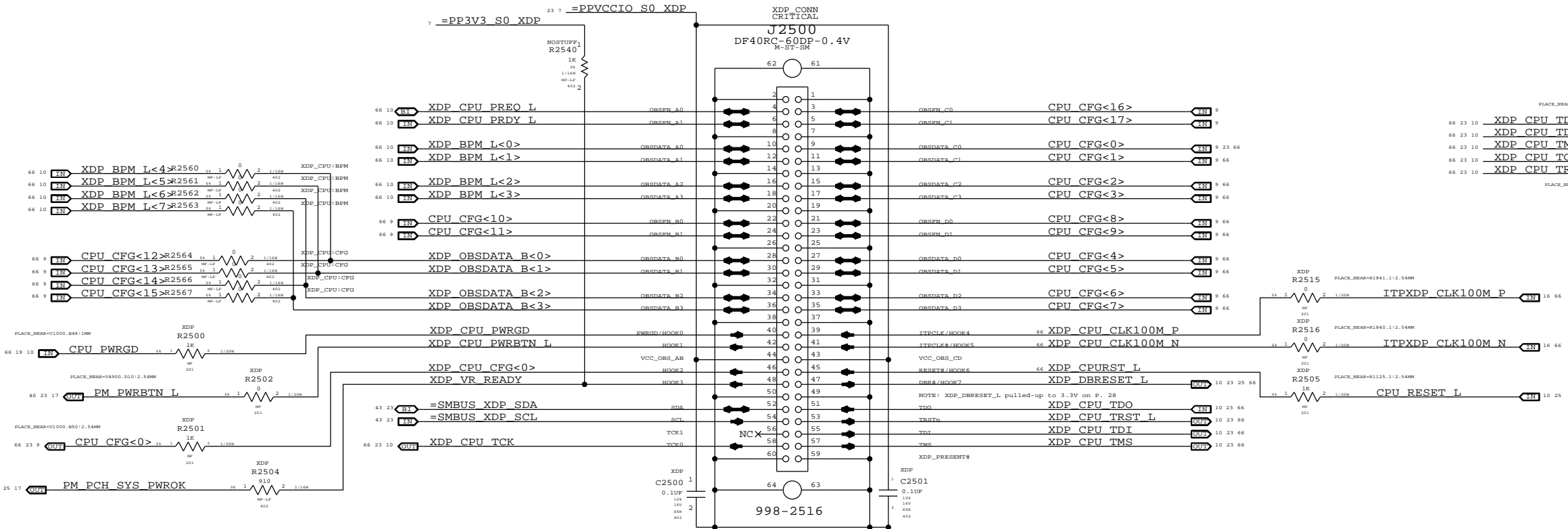
A

D

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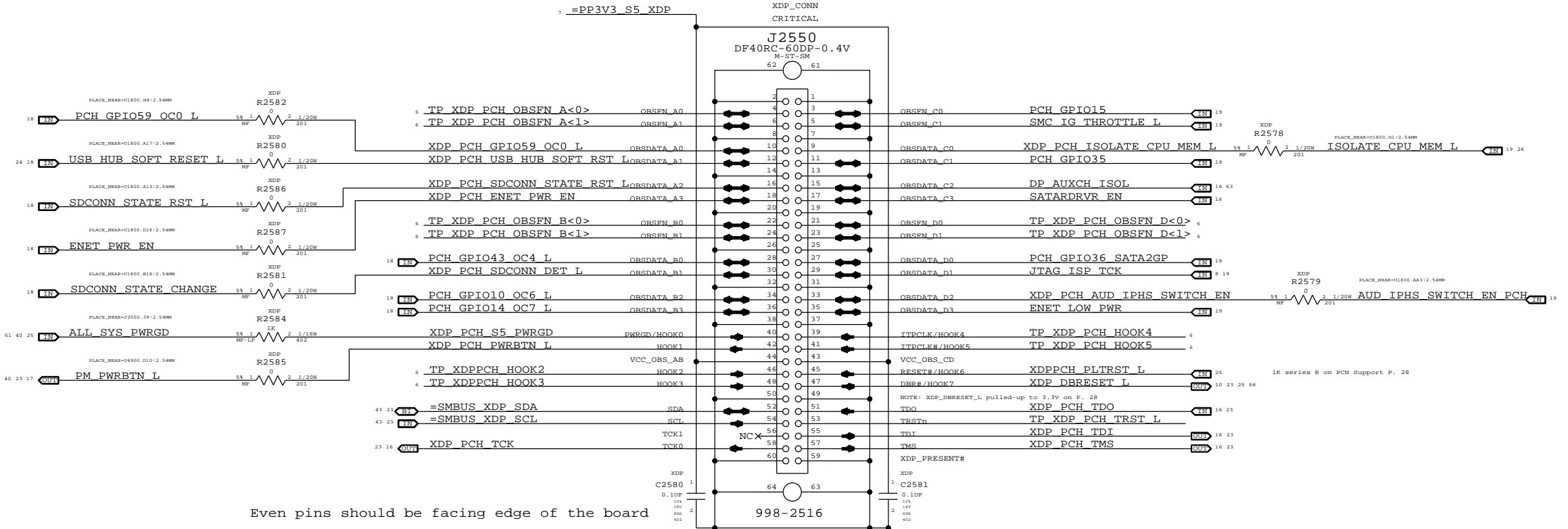


Even pins should be facing edge of the board

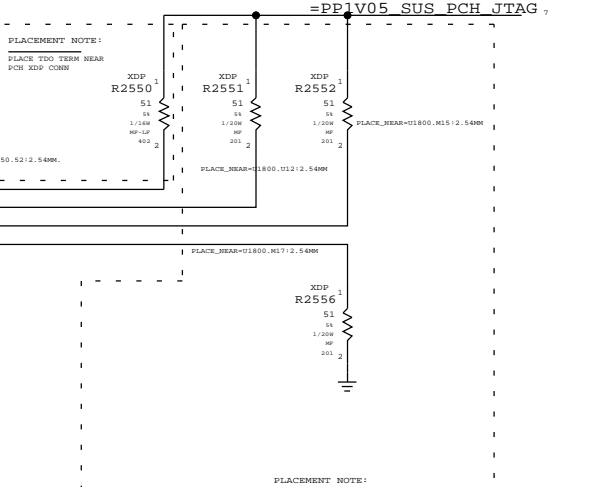
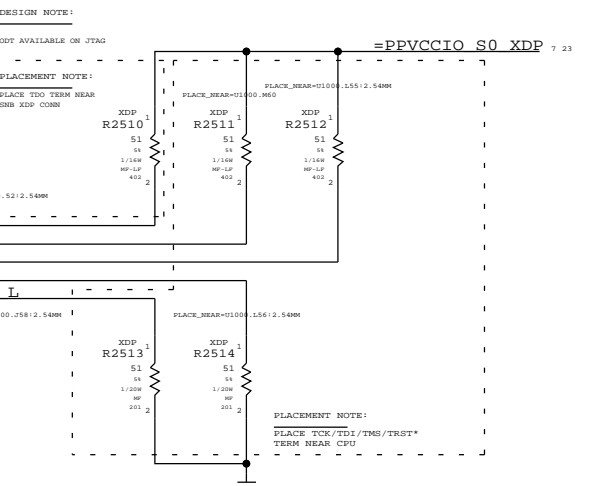
PCH MICRO2-XDP CONNECTOR


NOTE: This is not the standard XDP pinout

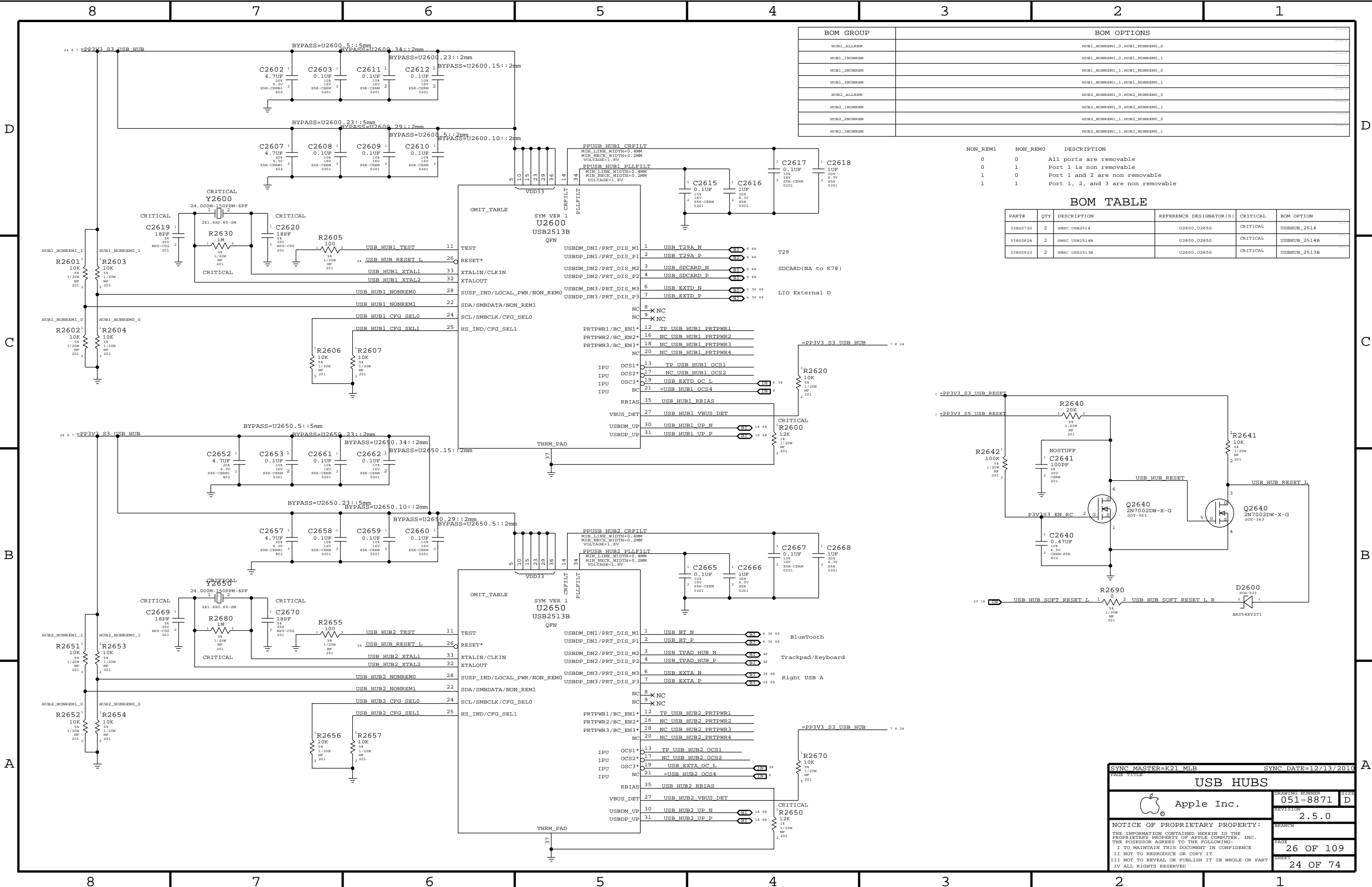
Use with 920-0782 Adapter Flex to support chipset debug



Even pins should be facing edge of the board



SYNC MASTER=K21 MLB		SYNC DATE=12/13/2010	
PAGE TITLE			
CPU & PCH XDP			
 Apple Inc.		DRAWING NUMBER	051-8871
		SIZE	D
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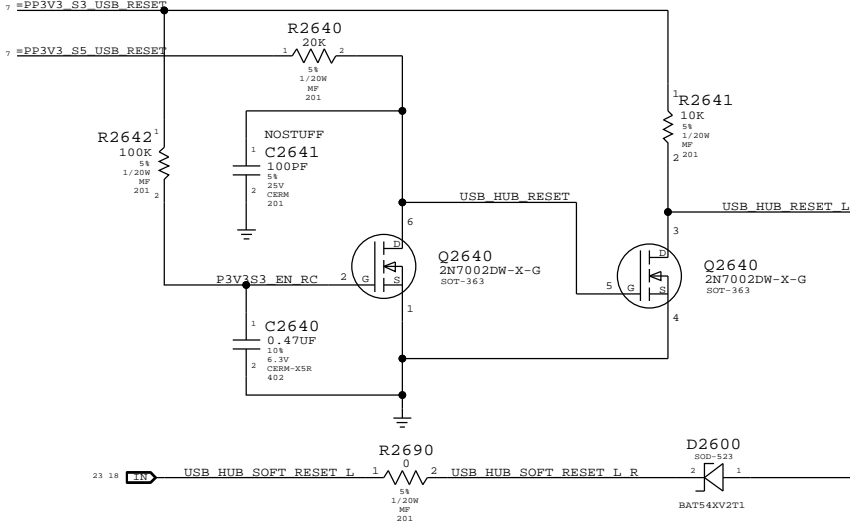


BOM GROUP	BOM OPTIONS
HUB1_ALLREM	HUB1_NONREM1_0,HUB1_NONREM0_0
HUB1_1NONREM	HUB1_NONREM1_0,HUB1_NONREM0_1
HUB1_2NONREM	HUB1_NONREM1_1,HUB1_NONREM0_0
HUB1_3NONREM	HUB1_NONREM1_1,HUB1_NONREM0_1
HUB2_ALLREM	HUB2_NONREM1_0,HUB2_NONREM0_0
HUB2_1NONREM	HUB2_NONREM1_0,HUB2_NONREM0_1
HUB2_2NONREM	HUB2_NONREM1_1,HUB2_NONREM0_0
HUB2_3NONREM	HUB2_NONREM1_1,HUB2_NONREM0_1

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
33850720	2	SMSC USB2514	U2600,U2650	CRITICAL	USBHUB_2514
33850824	2	SMSC USB2514B	U2600,U2650	CRITICAL	USBHUB_2514B
33850923	2	SMSC USB2513B	U2600,U2650	CRITICAL	USBHUB_2513B



SYNC MASTER=K21 MLB

SYNC DATE=12/13/2010

Apple Inc.

051-8871

2.5.0

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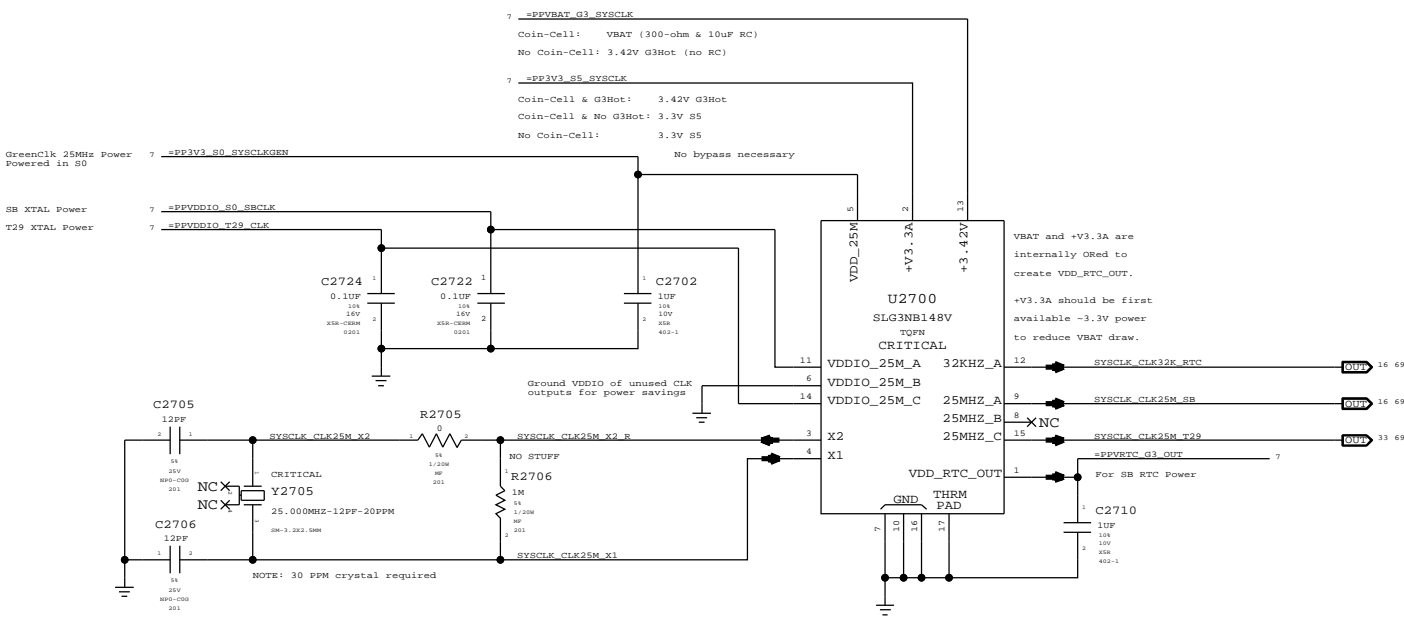
System RTC Power Source & 32kHz / 25MHz Clock Generator

D

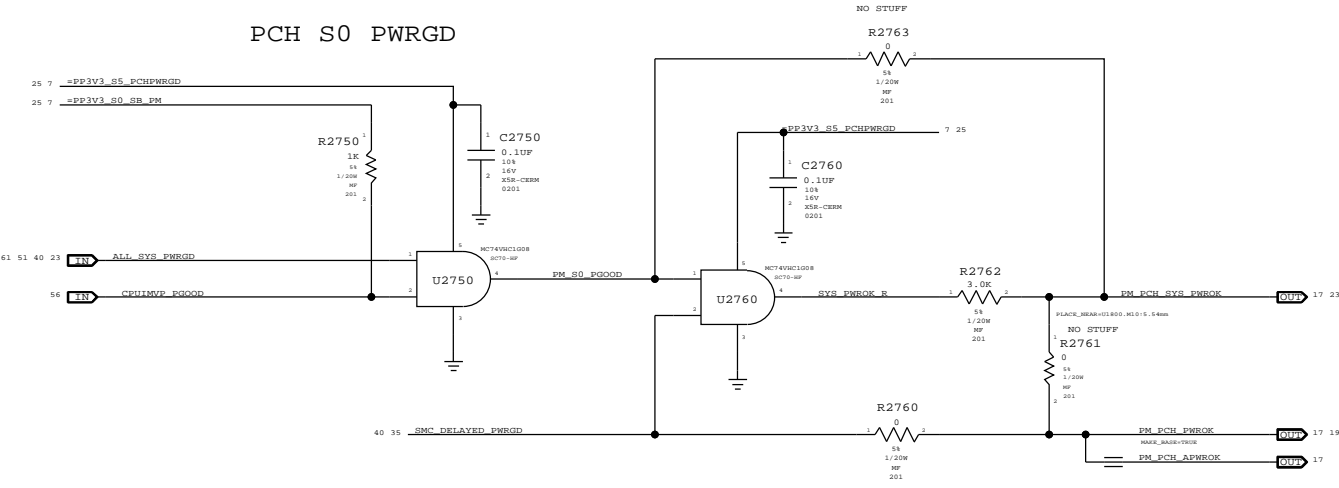
C

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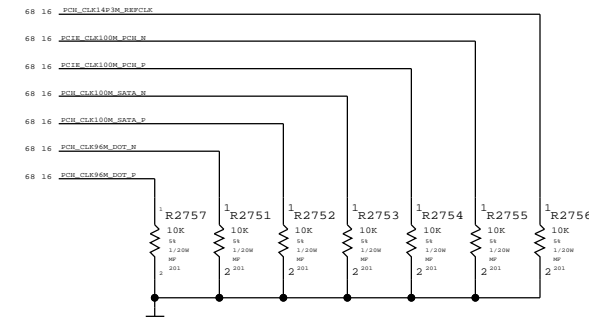


PCH S0 PWRGD



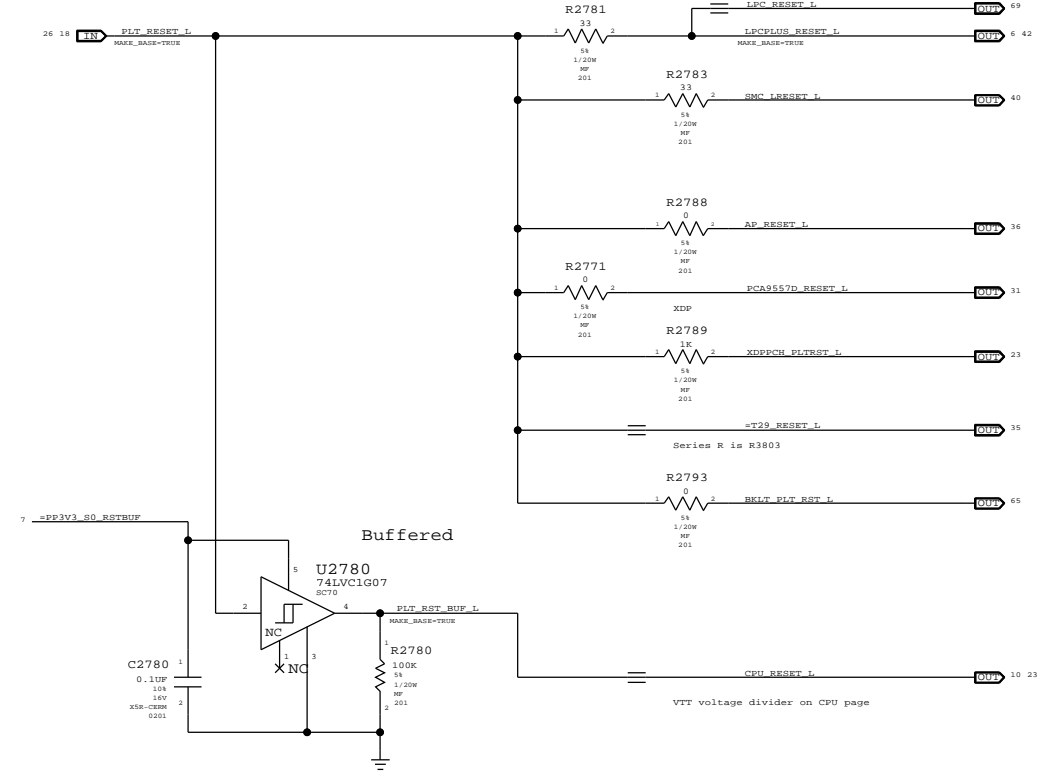
CLOCK (CK505)

UNUSED clock terminations for PCIM MODE

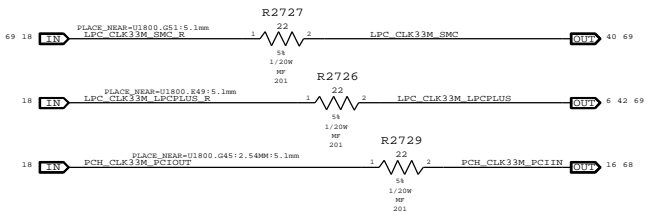
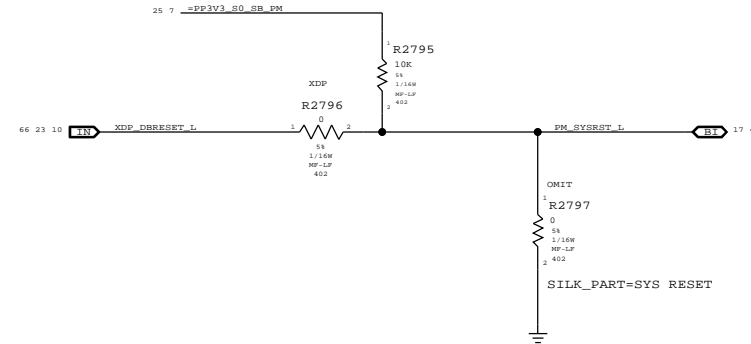


Platform Reset Connections

Unbuffered



PCH Reset Button

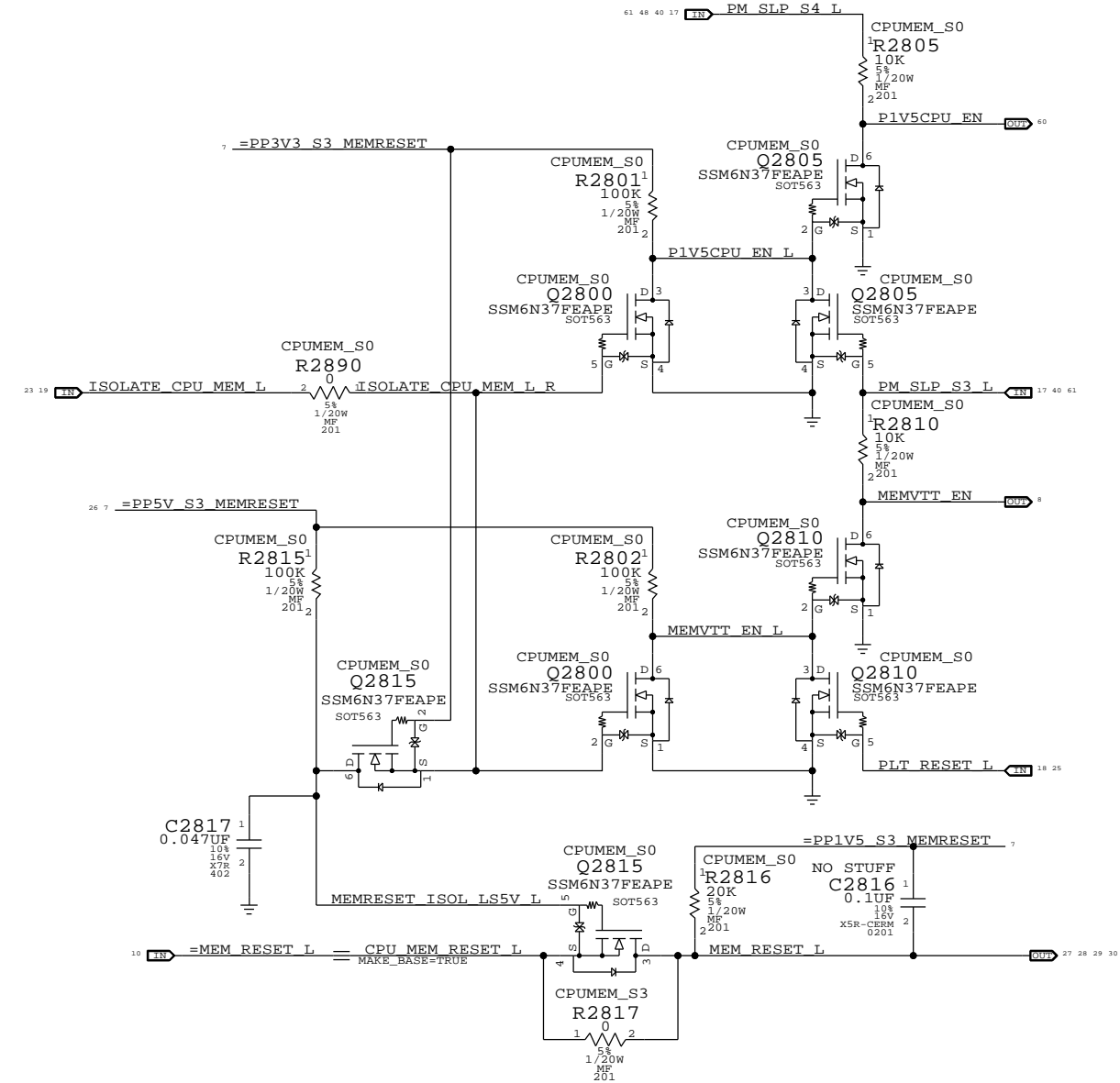


Clock (CK505) and Chipset Support	
Apple Inc.	DRAWING NUMBER 051-8871
REVISION 2.5.0	SIZE D
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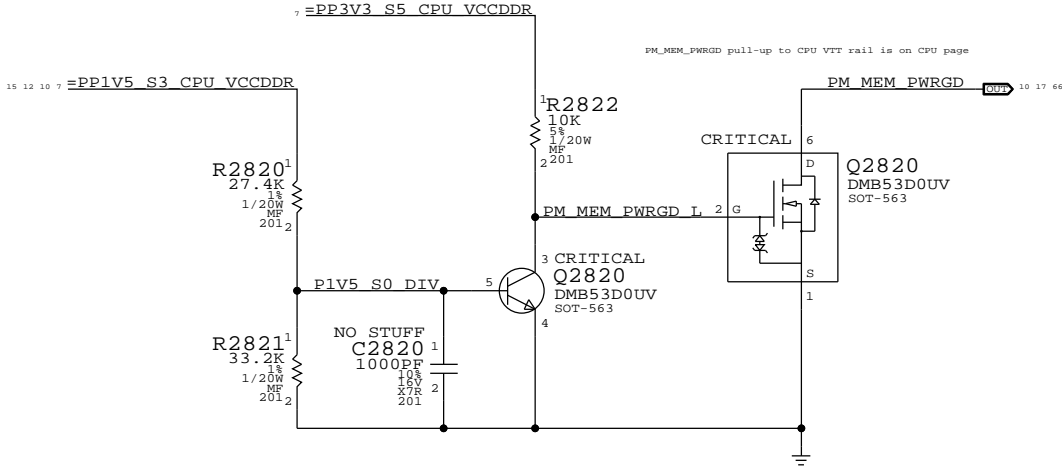
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the S0-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L

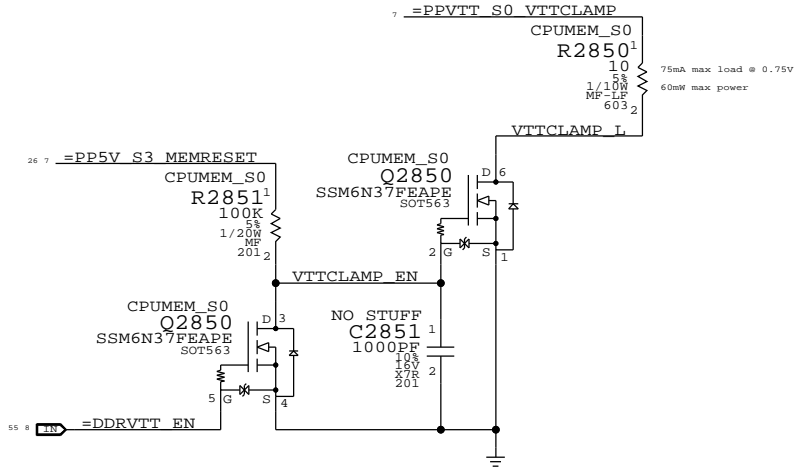


1V5 S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3



Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	CPU_MEM_RESET_L	1	1
1	0	1	1	1	1		1	1
to	2	0	0	1	1		0	1
3	0	0	0	1	X		0	0
S3	4	0	0	1	X		0	1
5	0	1	1	1	0 (*)		1	1
6	0	1	1	1	1		1	1
to	7	1	1	1	1	CPU_MEM_RESET_L	1	1
S0								

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

CPU Memory S3 Support



Apple Inc.

DRAWING NUMBER 051-8871

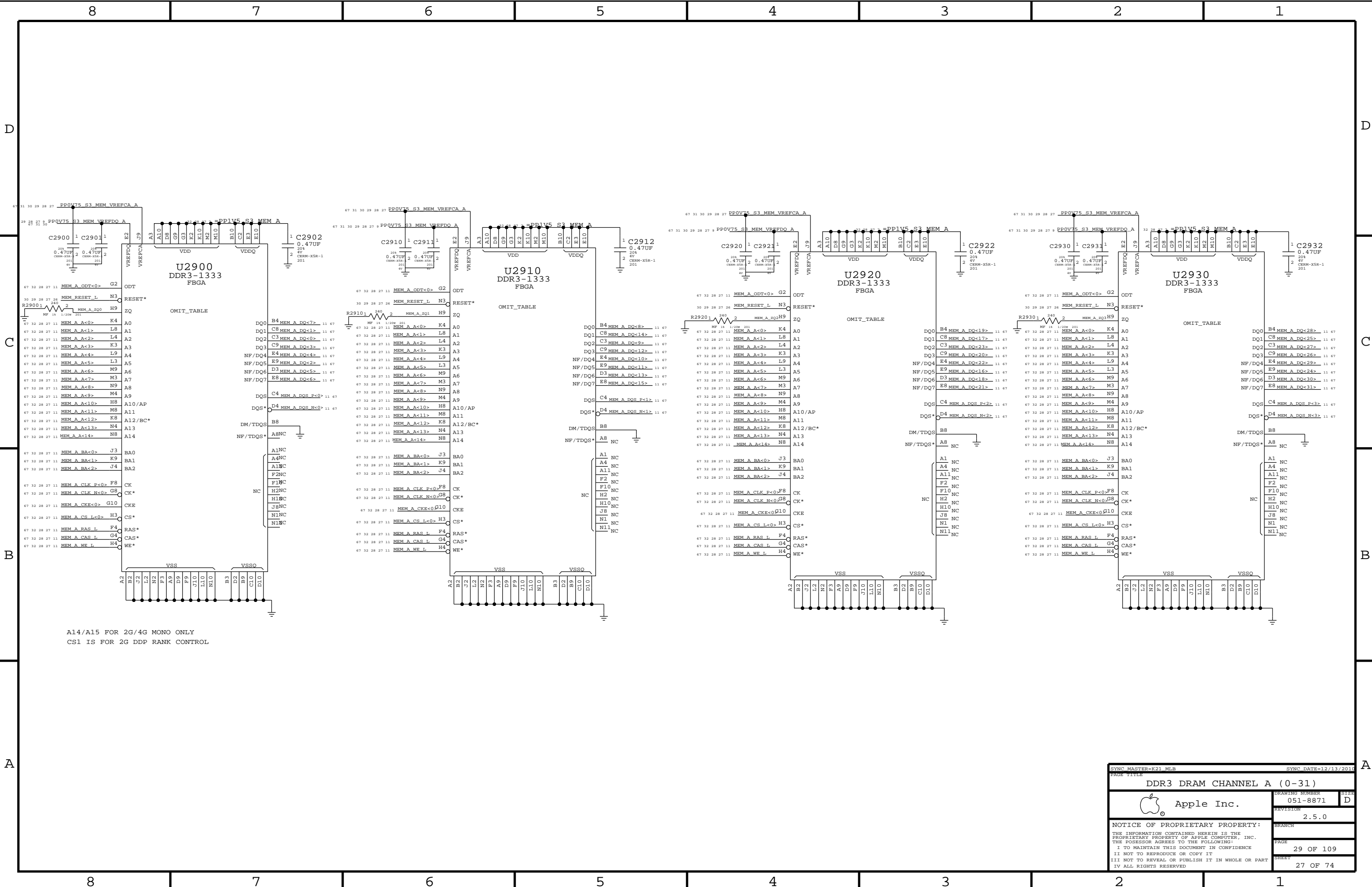
REVISION 2.5.0

BRANCH

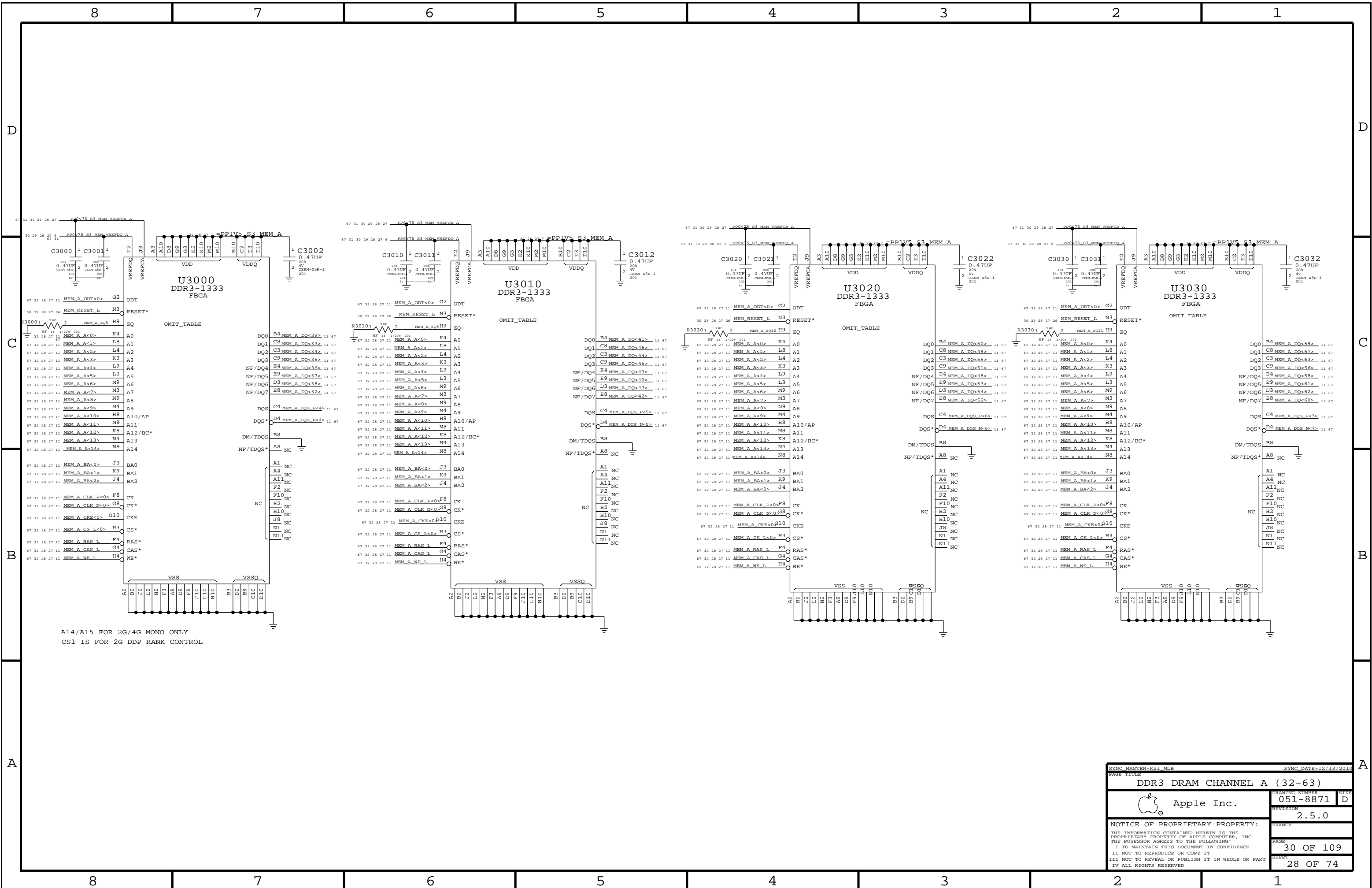
PAGE 28 OF 109

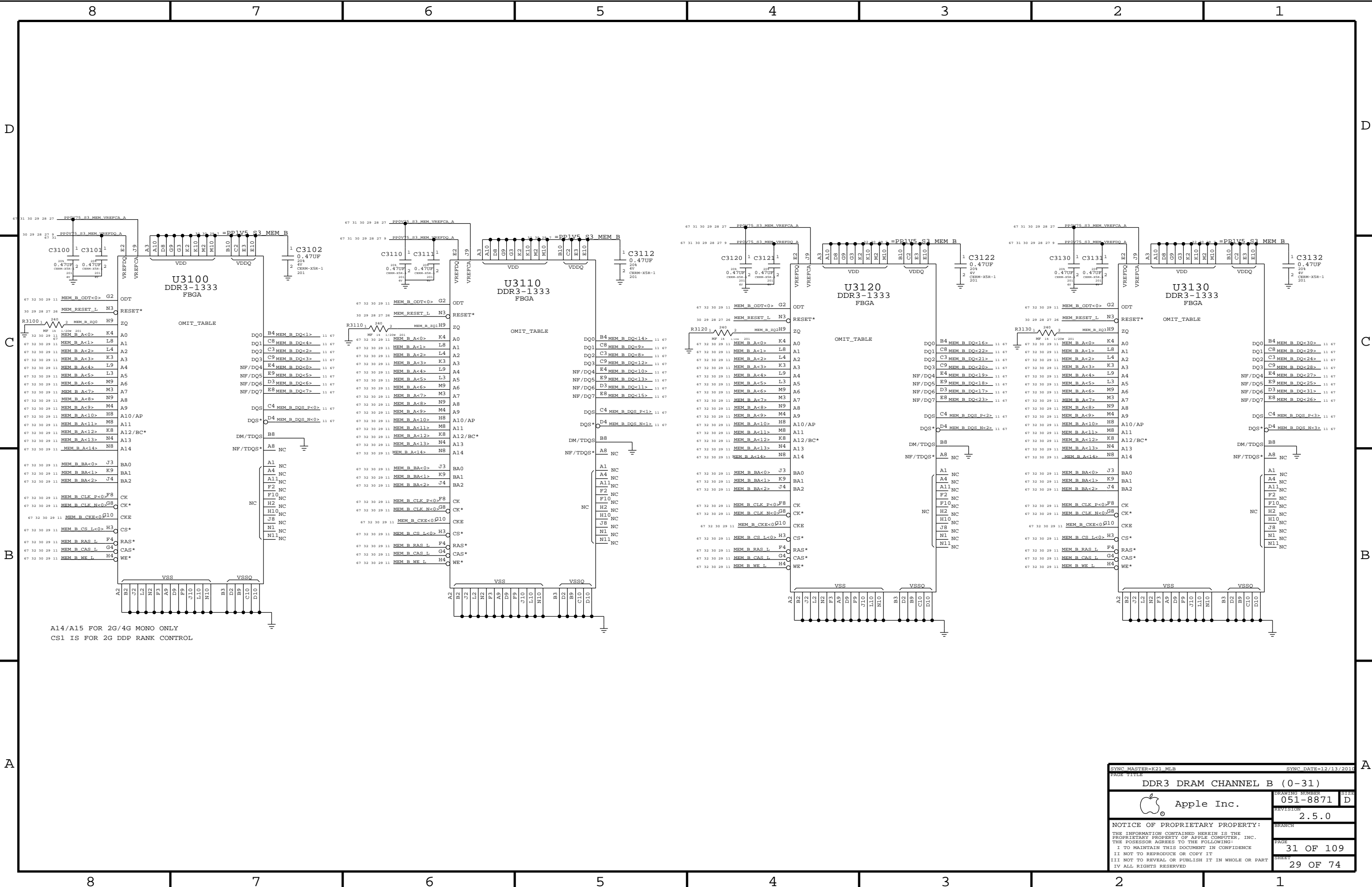
SHEET 26 OF 74

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


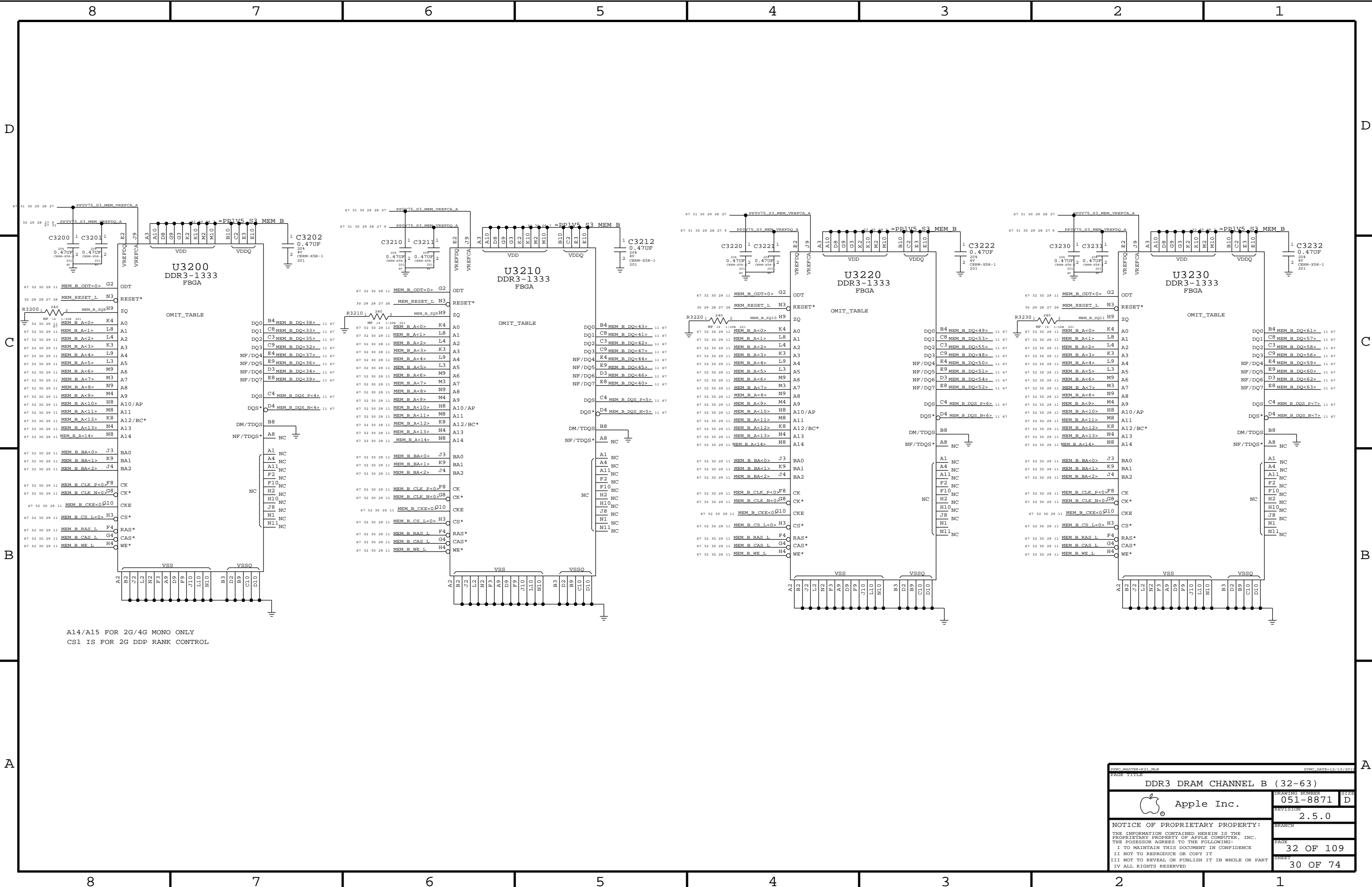
A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL






A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL

SYNC MASTER=K21 MLB		SYNC DATE=12/13/2010	
PAGE TITLE			
DDR3 DRAM CHANNEL B		(0-31)	
 Apple Inc.	DRAWING NUMBER	051-8871	SIZE D
	REVISION	2.5.0	
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SYMC PART#K11.MEM		SYMC DATE=12/13/2011	
PAGE TITLE			
DDR3 DRAM CHANNEL B (32-63)			
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	REVISION	2.5.0	
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		PAGE	32 OF 109
		SHEET	30 OF 74

D

C

B

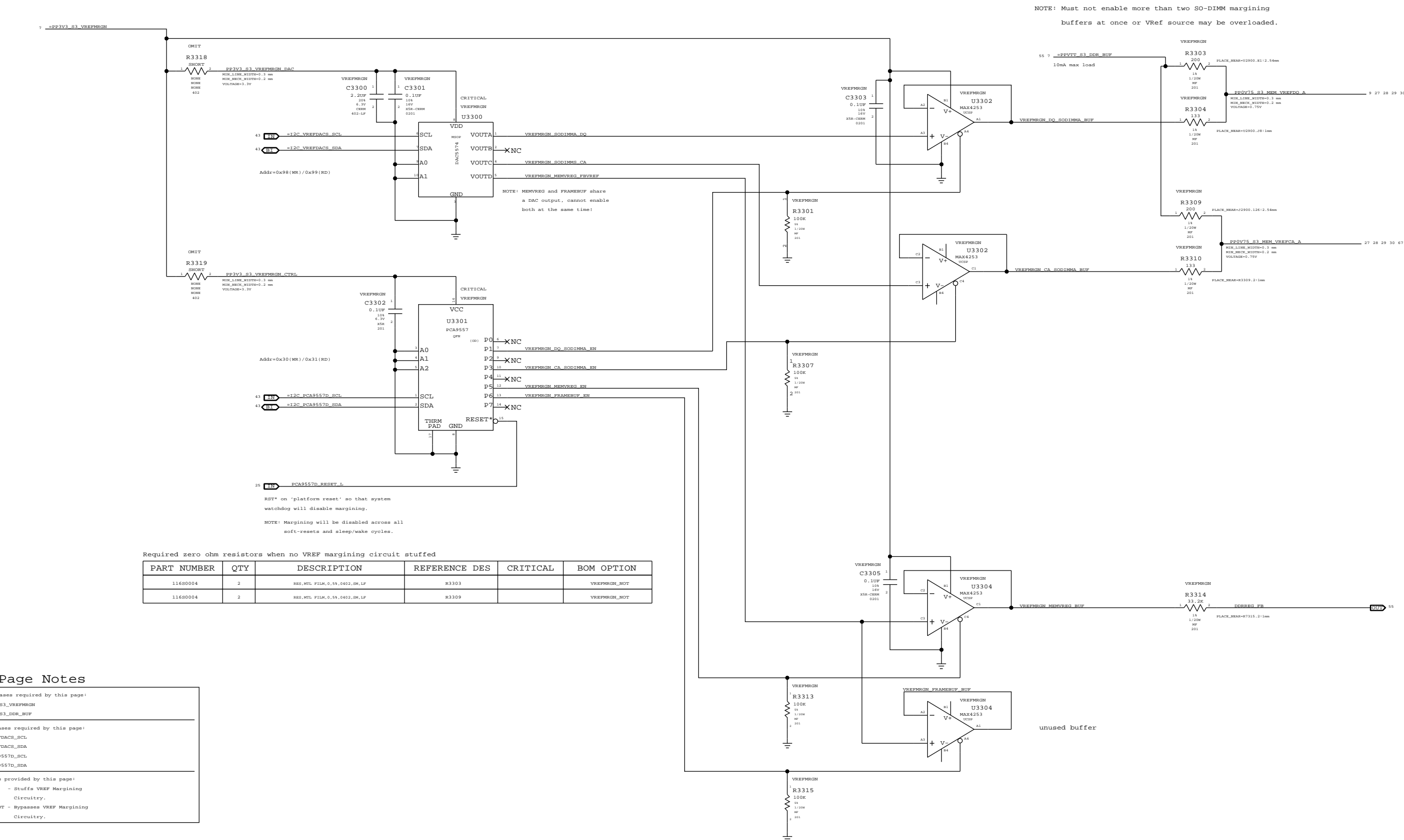
A

D

C

B

A



Page Notes

Power aliases required by this page:

- =PP3V3_S3_VREFMARGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:

- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:

- VREFMARG - Stuffs VREF Margining Circuitry.
- VREFMARG_NOT - Bypasses VREF Margining Circuitry.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% Vref)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4		
Nominal value		0.75V (DAC: 0x3A)			1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:		0.300V - 1.200V (+/- 450mV)			1.998V - 1.002V (+/- 498mV)	1.056V - 1.442V (+/- 180mV)
DAC range:		0.000V - 1.501V (0x00 - 0x74)			0.000V - 1.501V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:		+3.4mA - -3.4mA (- = sourced)			+33uA - -33uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:		7.69mV / step @ output			8.59mV / step @ output	1.51mV / step @ output

SYMC PARTNERSHIP MCB

SYMC DATE=12/13/2015

PAGE TITLE

FSB/DDR3/FRAMEBUF Vref Margining

Apple Inc.

DRAWING NUMBER
051-8871

REVISION
2.5.0

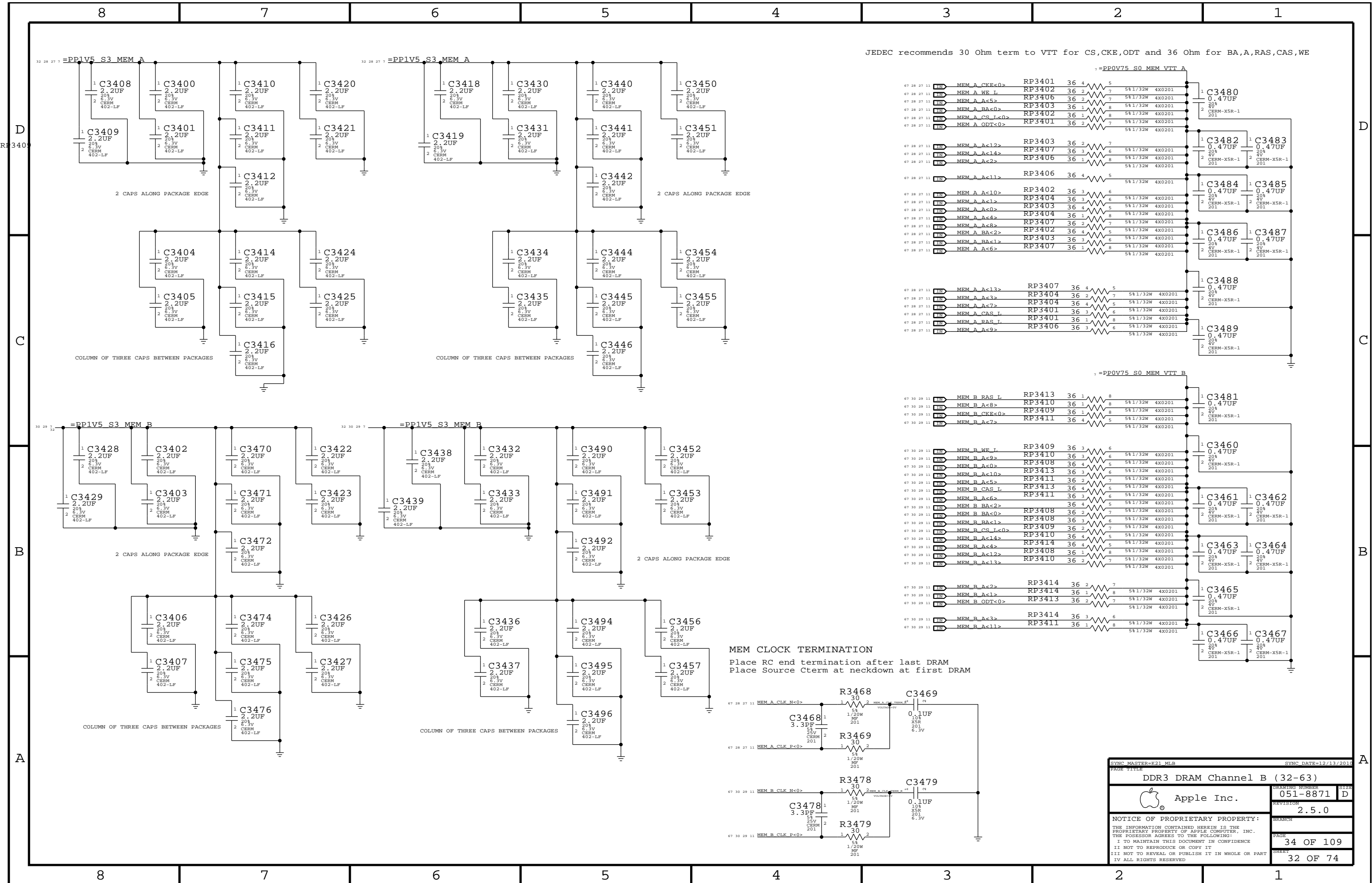
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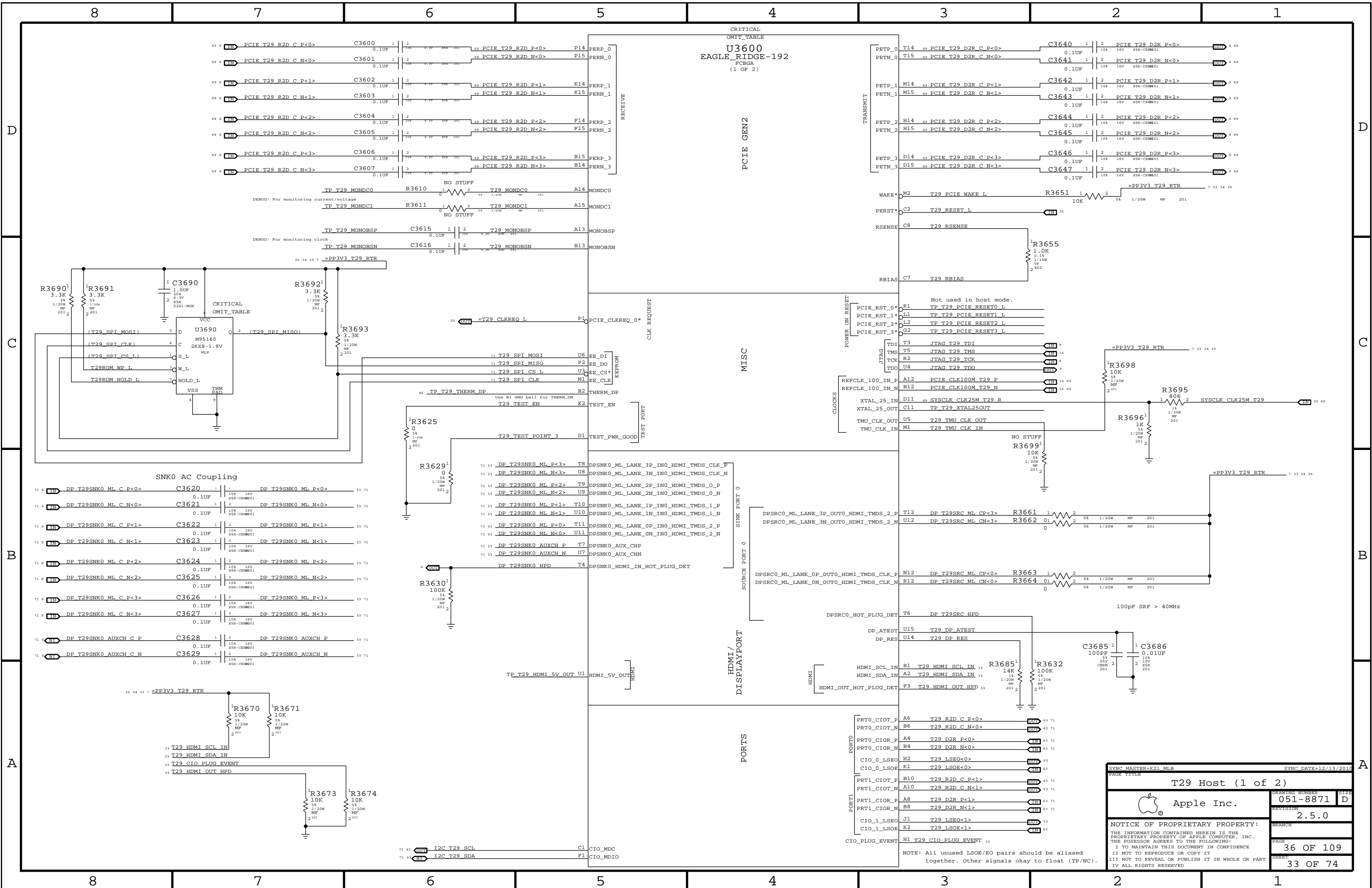
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SYNC MASTER=K21 MLB		SYNC DATE=12/13/2016	
PAGE TITLE			
DDR3 DRAM Channel B (32-63)			
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	REVISION	2.5.0	
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PAGE	34 OF 109		
SHEET	32 OF 74		



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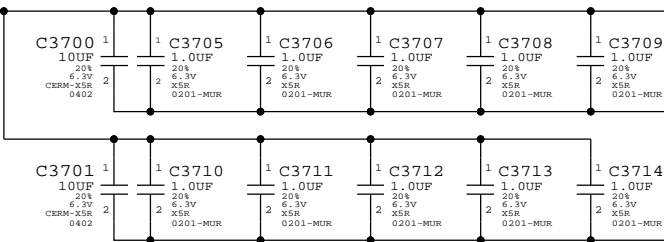
D

C

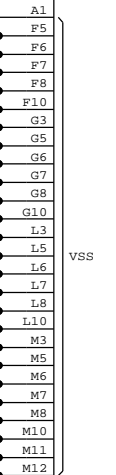
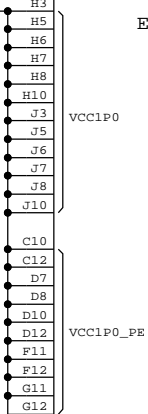
B

A

³⁴ 7 =PP1V05 T29_RTR
2100 mA (Single Port)
2250 mA (Dual Port)
EDP: 3000 mA

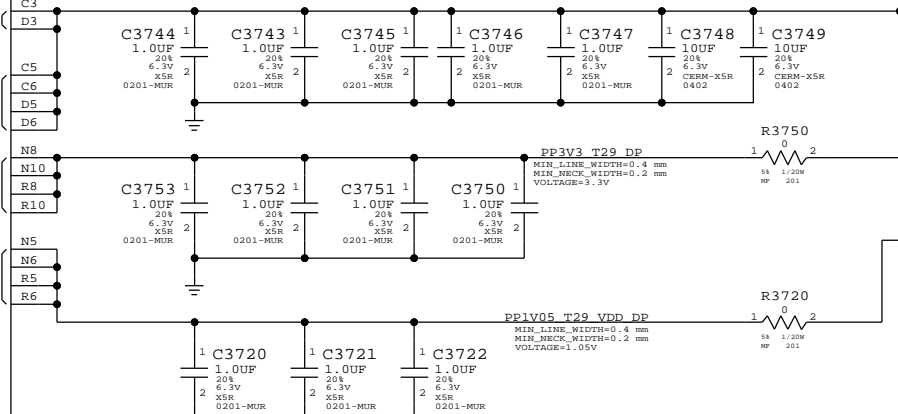
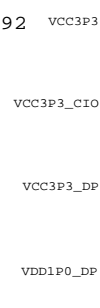


CRITICAL
OMIT_TABLE
U3600
EAGLE_RIDGE-192
FCBGA
(2 OF 2)



VCC

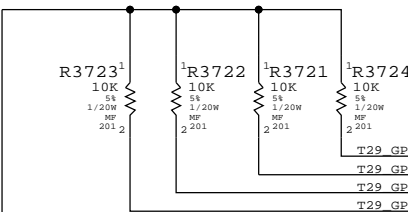
GND



=PP3V3 T29_RTR
135 mA (Single-Port)
152 mA (Dual-Port)
EDP: 200 mA

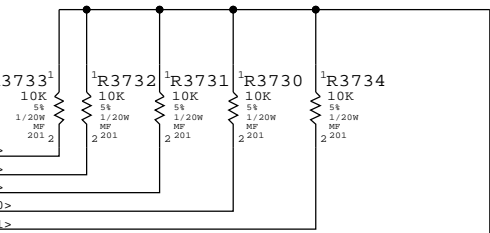
0-ohms are placeholders for now, replace with proper values after characterization.

=PP1V05 T29_RTR
2100 mA (Single Port)
2250 mA (Dual Port)
EDP: 3000 mA




T29_GPIO<0>
T29_GPIO<4>
T29_GPIO<5>
T29_GPIO<6>

GPIO_7
GPIO_8
GPIO_9
GPIO_10
GPIO_11



T29_GPIO<7>
T29_GPIO<8>
T29_GPIO<9>
T29_GPIO<10>
T29_GPIO<11>

SYNC MASTER=K21 MLB		SYNC DATE=12/13/2010	
PAGE TITLE			
T29 Host (2 of 2)			
	DRAWING NUMBER		SIZE
	051-8871		D
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		2.5.0	
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BRANCH		PAGE	
		37 OF 109	
SHEET		34 OF 74	

Page Notes

Power aliases required by this page:

- PPVIN_SW_T29BST (8-13V Boost Input)
- PP18V_T29_REG (18V Boost Output)
- PP3V3_T29_P3V3T29FET (3.3V FET Input)
- PP3V3_T29_FET (3.3V FET Output)
- PP3V3_S0_T29PWRCTL
- PP1V05_T29_P1V05T29FET (1.05V FET Input)
- PP1V05_T29_FET (1.05V FET Output)

Signal aliases required by this page:

- T29_CLKREQ_L
- T29_RESET_L

BOM options provided by this page:

T29BST:Y - Stuffs 18V boost circuitry.

T29 18V Boost Regulator

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 46mOhm @ 4.5V Vgs
Id(max): 3.7A @ 70C

CRITICAL
T29BST:Y
Q3880
SI8409DB
BGA

CRITICAL
T29BST:Y
L3895
6.8UH-4.0A
PIMB062D-SM

CRITICAL
T29BST:Y
D3895
POWERDI-123
DFLS230L

D

D

C

C

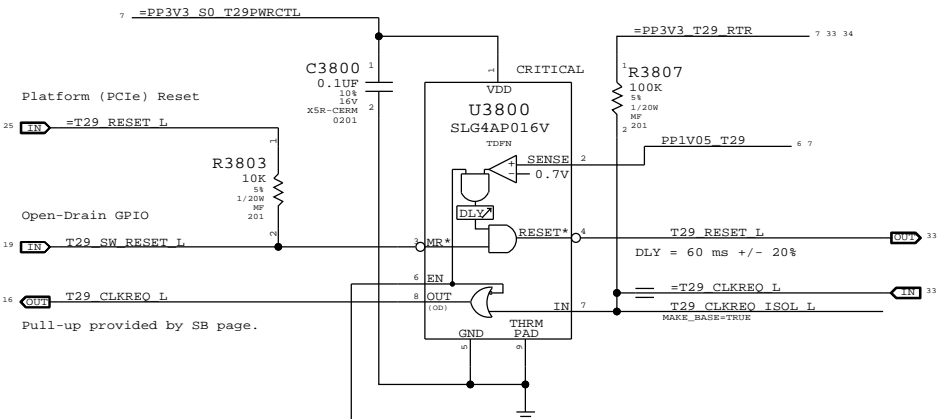
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B

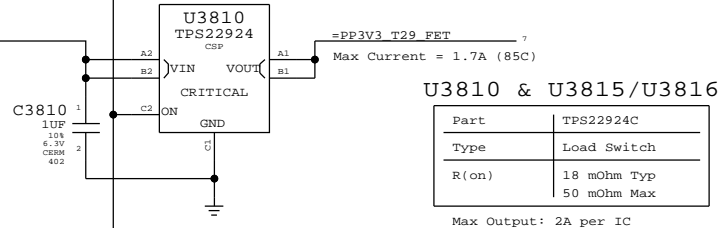
A

A

Supervisor & CLKREQ# Isolation



3.3V T29 Switch

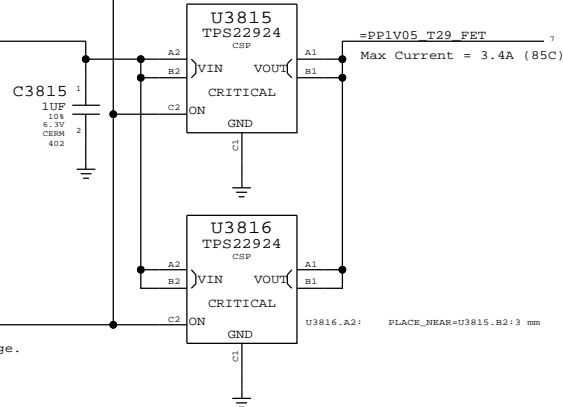



U3810 & U3815/U3816

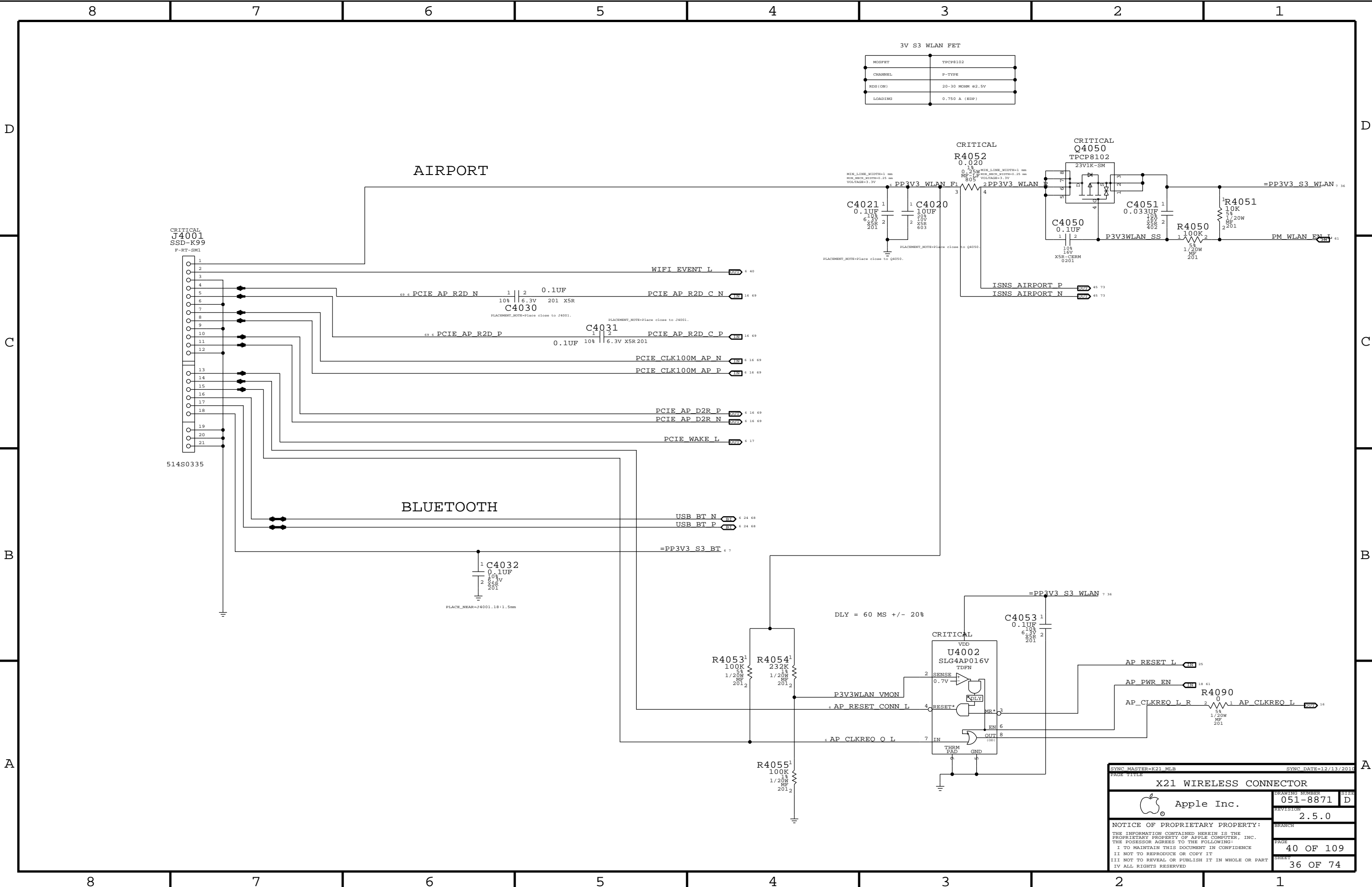
Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

Max Output: 2A per IC

1.05V T29 Switch



SYNC MASTER-K21 MLB		SYNC DATE-12/13/2010	
PAGE TITLE			
T29 Power Support			
 Apple Inc.	DRAWING NUMBER	051-8871	SIZE D
	REVISION	2.5.0	
	BRANCH		
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		PAGE	38 OF 109
		SHEET	35 OF 74



3V S3 WLAN FET	
MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	20-30 MOHM @2.5V
LOADING	0.750 A (RDP)

SYNC MASTER=X21 MLB

SYNC DATE=12/13/2010

X21 WIRELESS CONNECTOR

Apple Inc.

051-8871

2.5.0

40 OF 109

36 OF 74

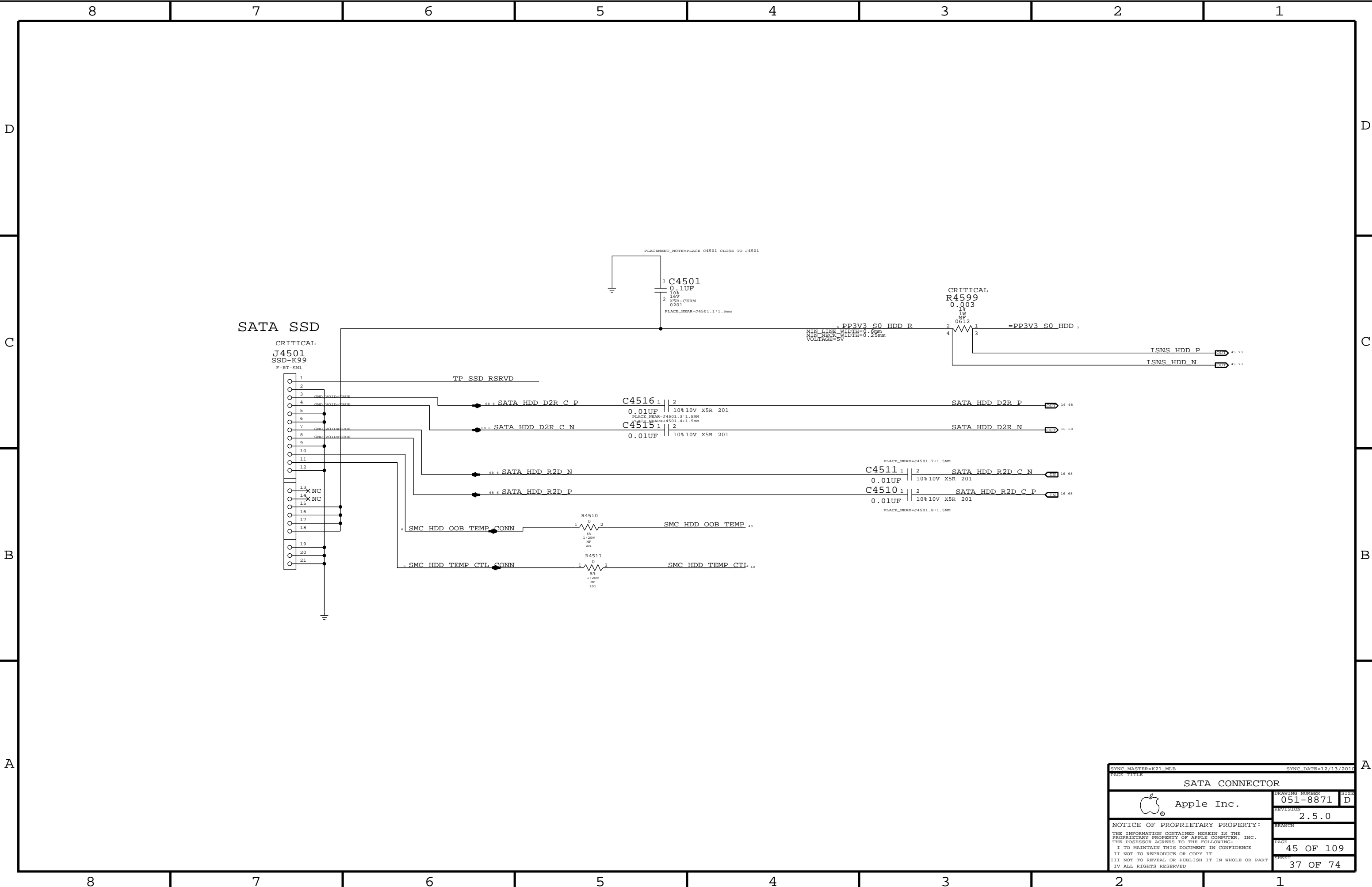
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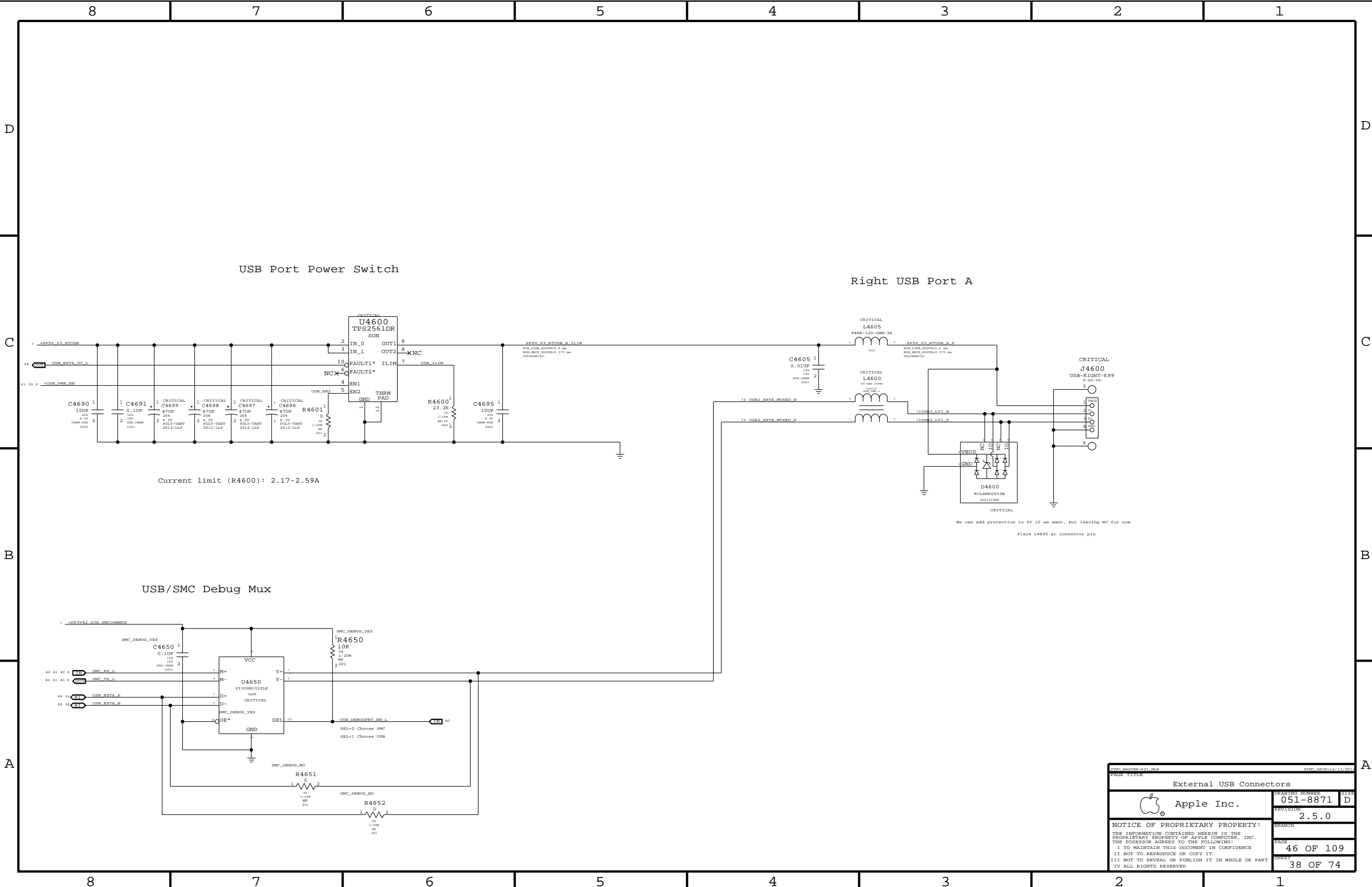
II NOT TO REPRODUCE OR COPY IT

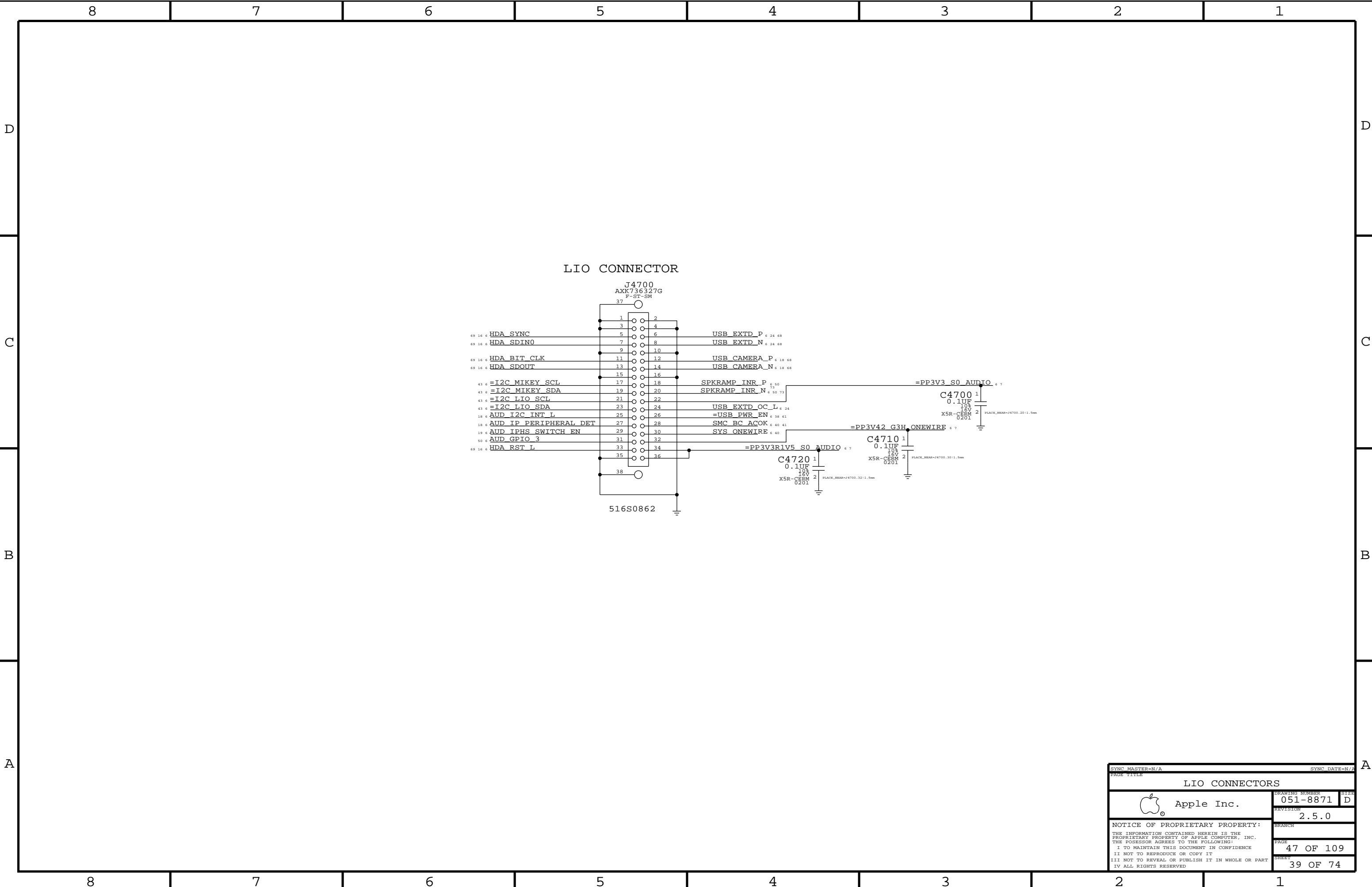
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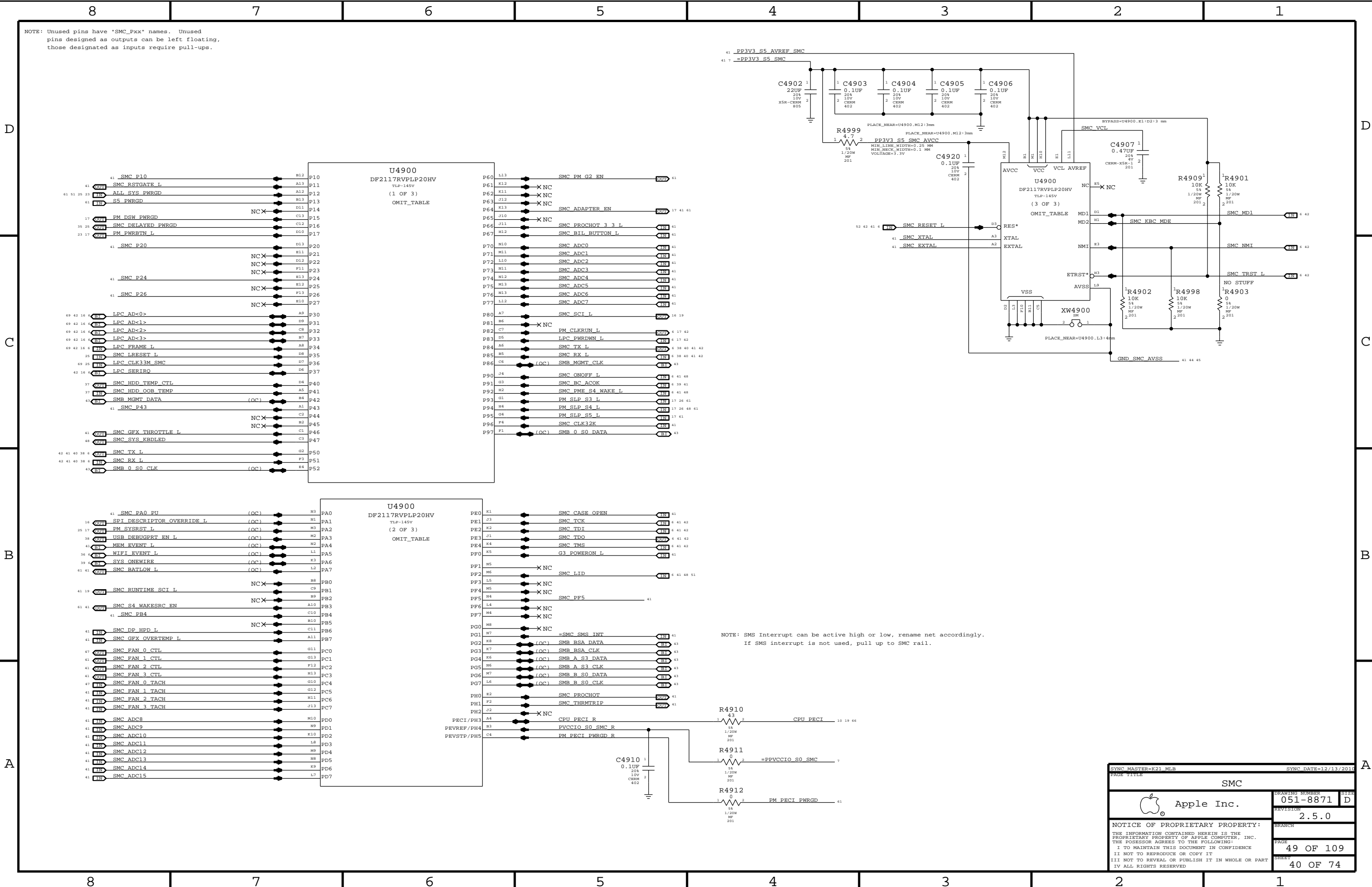
IV ALL RIGHTS RESERVED



SYNC MASTER=K21 MLB		SYNC DATE=12/13/2010	
PAGE TITLE			
SATA CONNECTOR			
 Apple Inc.		DRAWING NUMBER	051-8871
		REVISION	2.5.0
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		PAGE	45 OF 109
		SHEET	37 OF 74




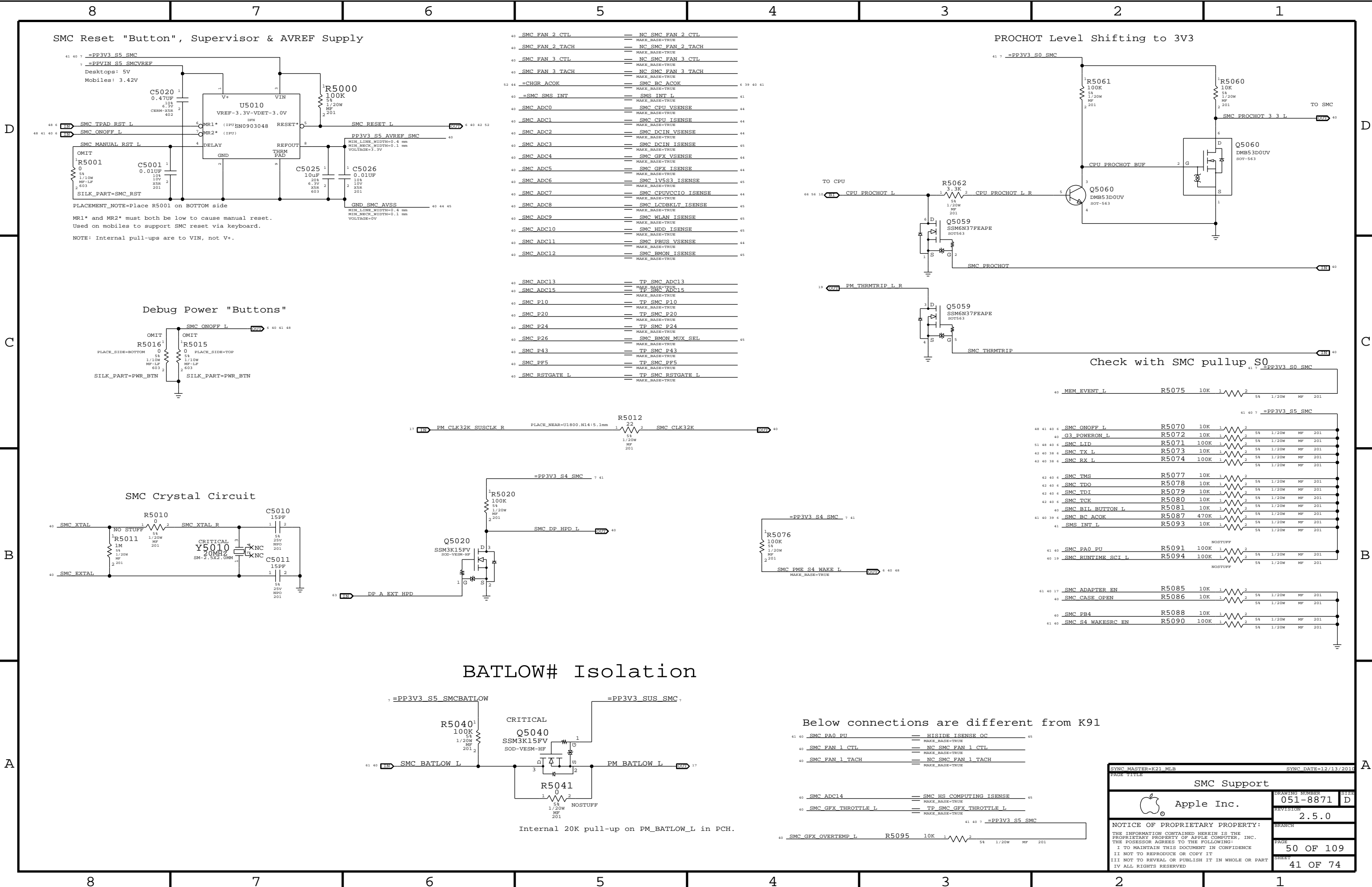


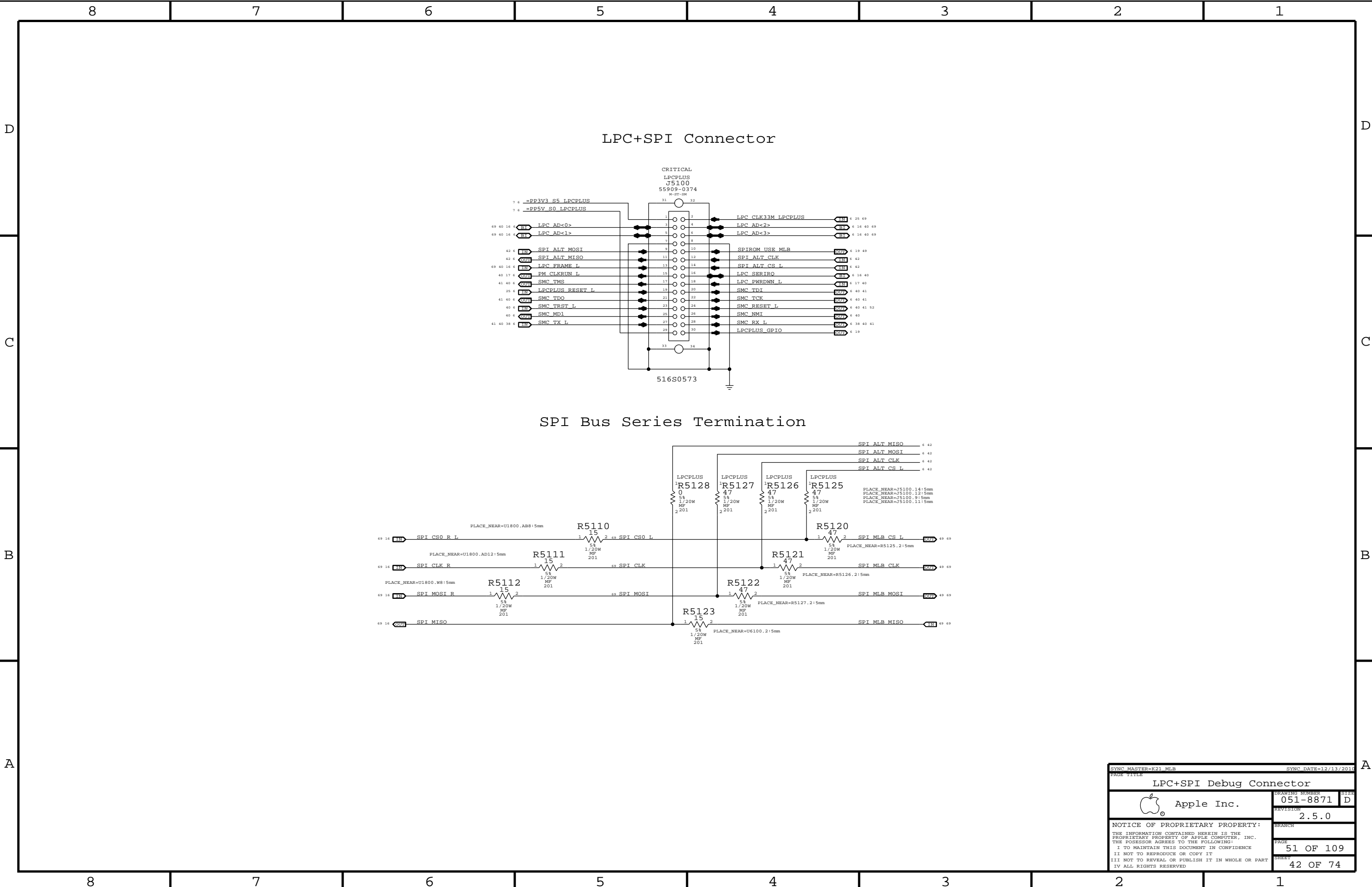


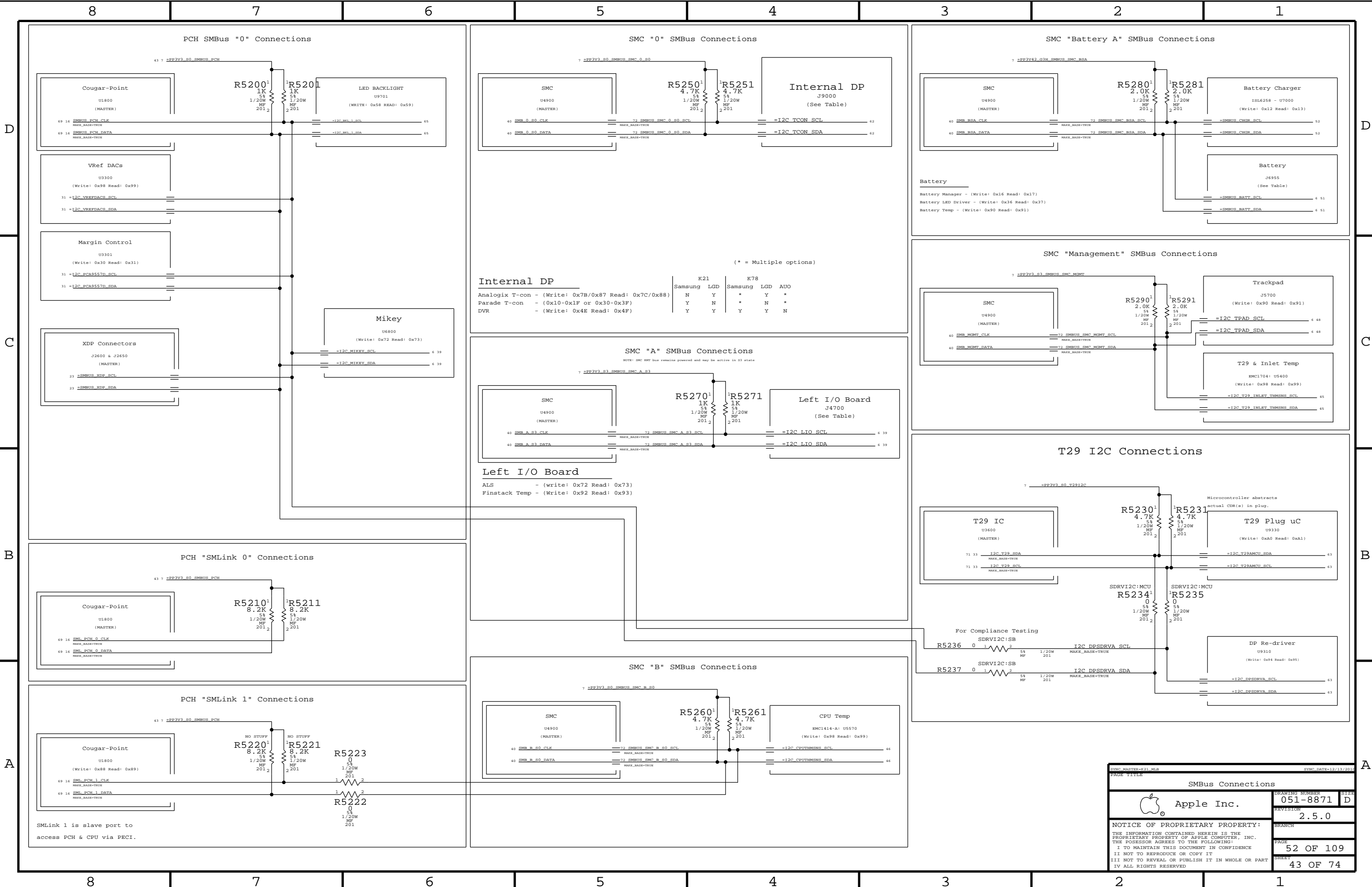
SYNC MASTER=K21 MLB

SYNC DATE=12/13/2010

SMC		DRAWING NUMBER	SIZE
 Apple Inc.		051-8871	D
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		2.5.0	49 OF 109
			40 OF 74







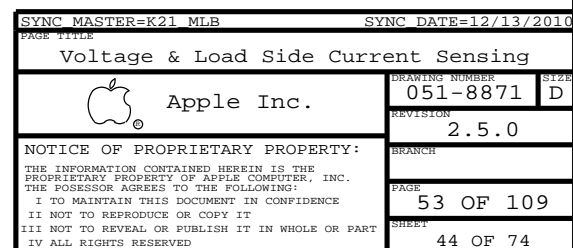
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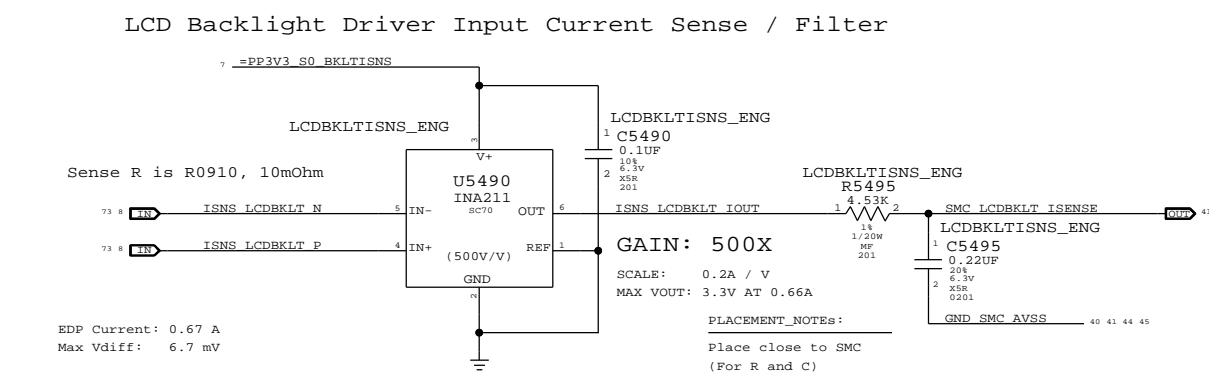
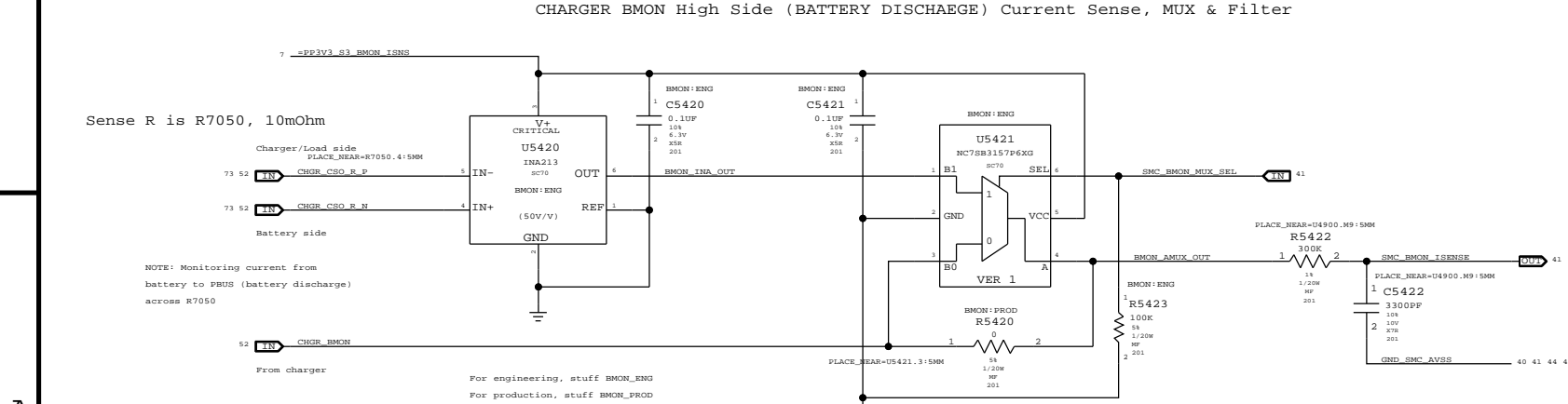
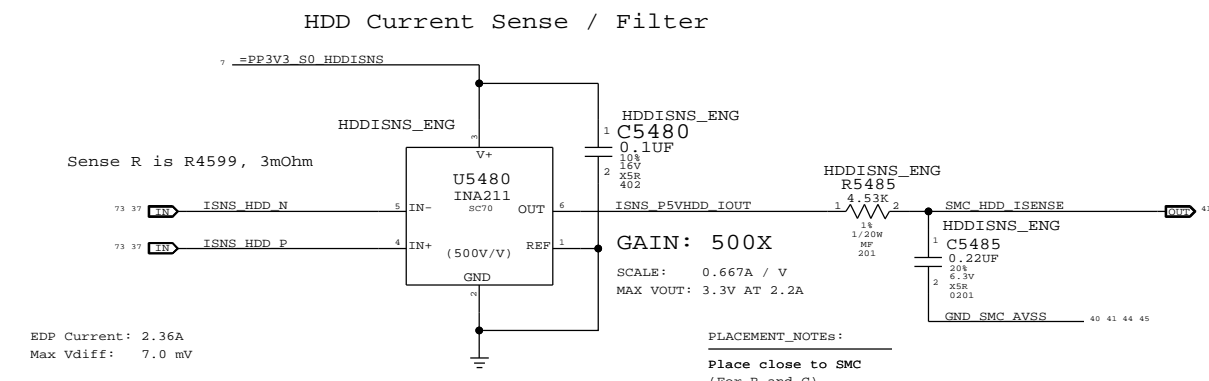
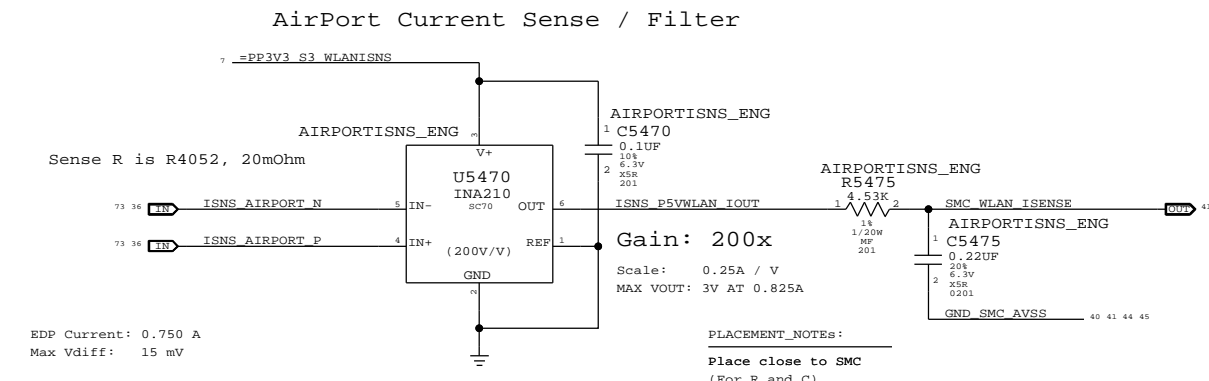
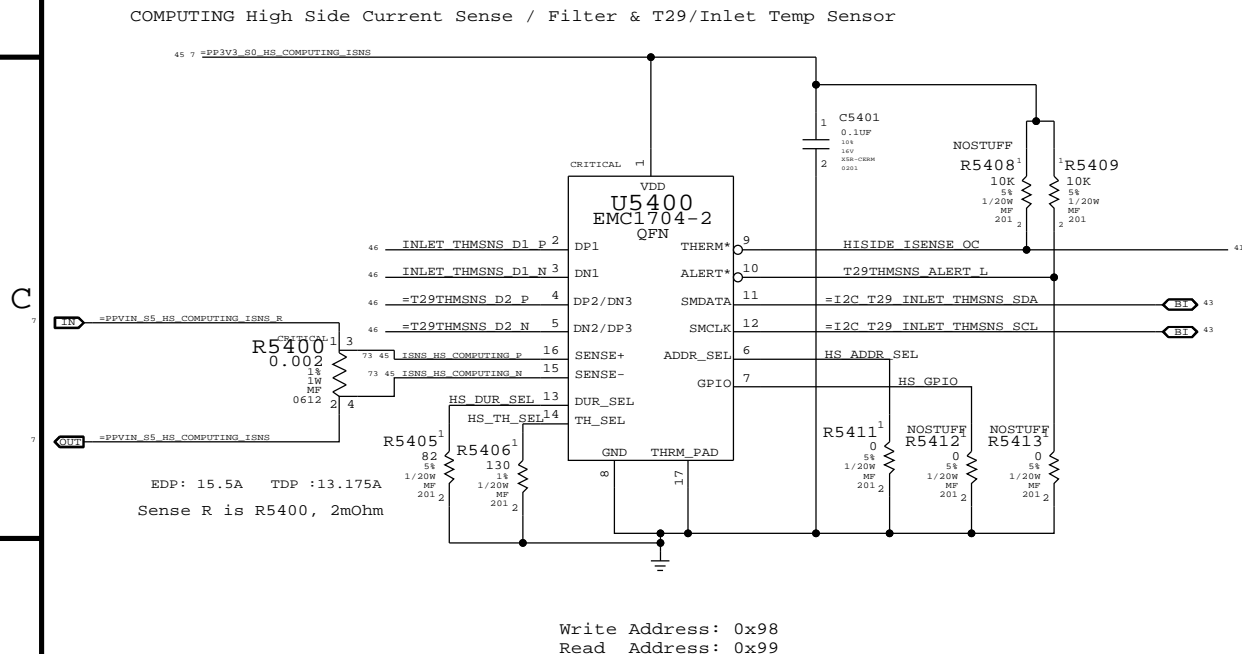
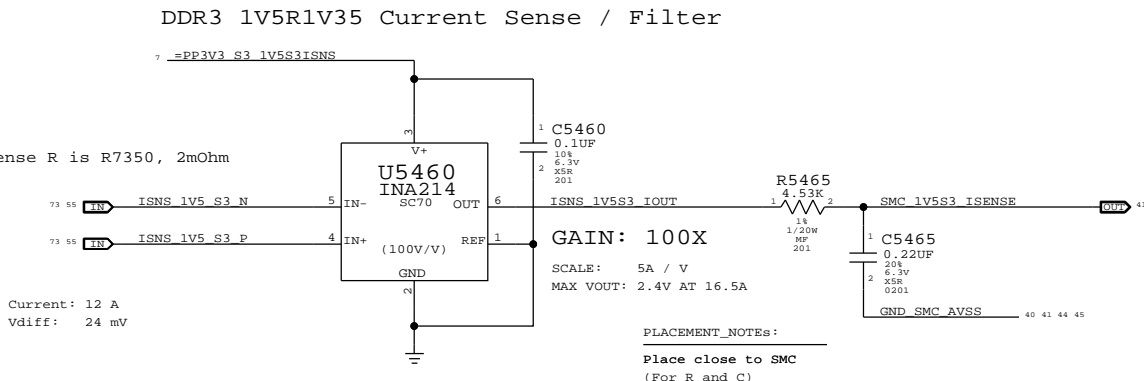
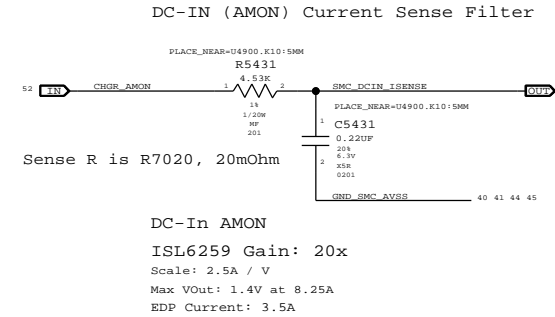
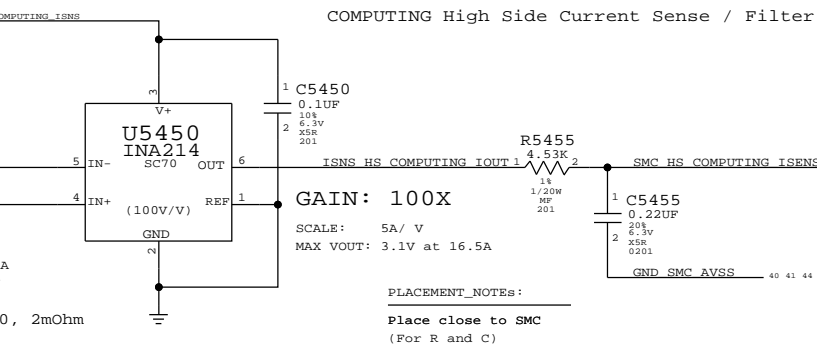
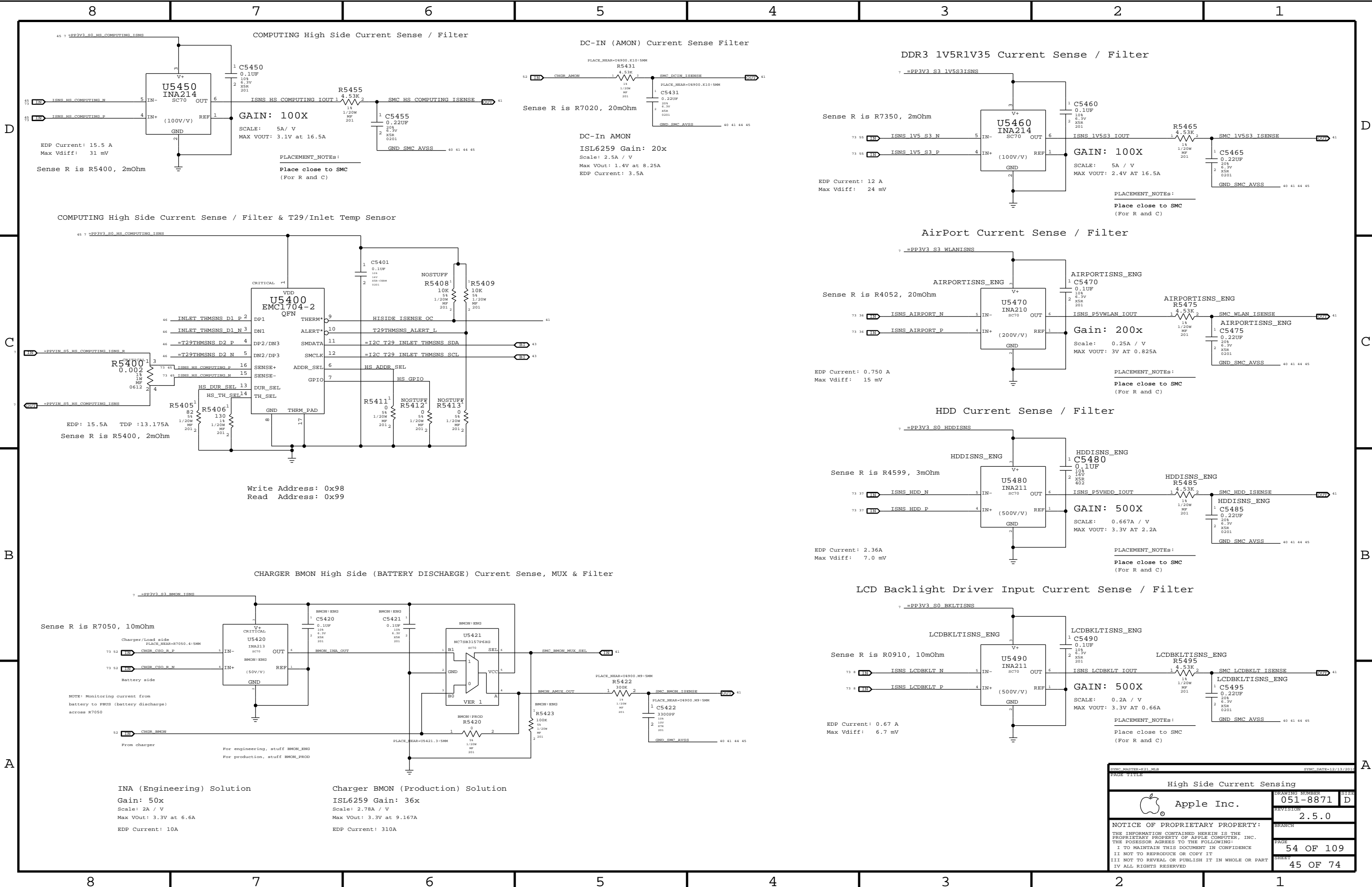


B



7 56 5

4



INA (Engineering) Solution

Gain: 50x

Scale: 2A / V

Max Vout: 3.3V at 6.6A

EDP Current: 10A


Charger BMON (Production) Solution

ISL6259 Gain: 36x

Scale: 2.78A / V

Max Vout: 3.3V at 9.167A

EDP Current: 310A

SYMC MASTER=K11 MCB		SYMC DATE=12/13/2016	
PAGE TITLE			
High Side Current Sensing			
	Apple Inc.	DRAWING NUMBER	051-8871
		SIZE	D
		REVISION	2.5.0
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		PAGE	54 OF 109
		SHEET	45 OF 74

CPU Proximity Sensor

Detect CPU Die Temperature

Detect DDR/5V/3.3V Proximity Temperature

T29 Die

Replacing caps with 100K PD on ISENSE SMC inputs

T29,MLB Bottom & Inlet Proximity Sensors

Placement note:
Place Q5510 next to DDR/5V/3.3V supply on TOP side

Placement note:
Place Q5530 between rear vent on bottom side

Placement note:
Place Q5520 close to T29 on TOP side

Placement note:
Place Q5540 on MLB bottom side opposite U5400

Part Number

Qty

Description

Reference Des

Critical

BOM Option

117S0008

1

RES,MF,1/20W,100K OHM,5,0201,SMD

C5361

VCCIOISNS_PROD

117S0008

1

RES,MF,1/20W,100K OHM,5,0201,SMD

C5475

AIRPORTISNS_PROD

117S0008

1

RES,MF,1/20W,100K OHM,5,0201,SMD

C5485

HDDISNS_PROD

117S0008

1

RES,MF,1/20W,100K OHM,5,0201,SMD

C5495

LCDCLKTISNS_PROD

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117S0008

1

RES,MF,1/20W,100K OHM,5,0201,SMD

C5475

AIRPORTISNS_PROD

117S0008

1

RES,MF,1/20W,100K OHM,5,0201,SMD

C5485

HDDISNS_PROD

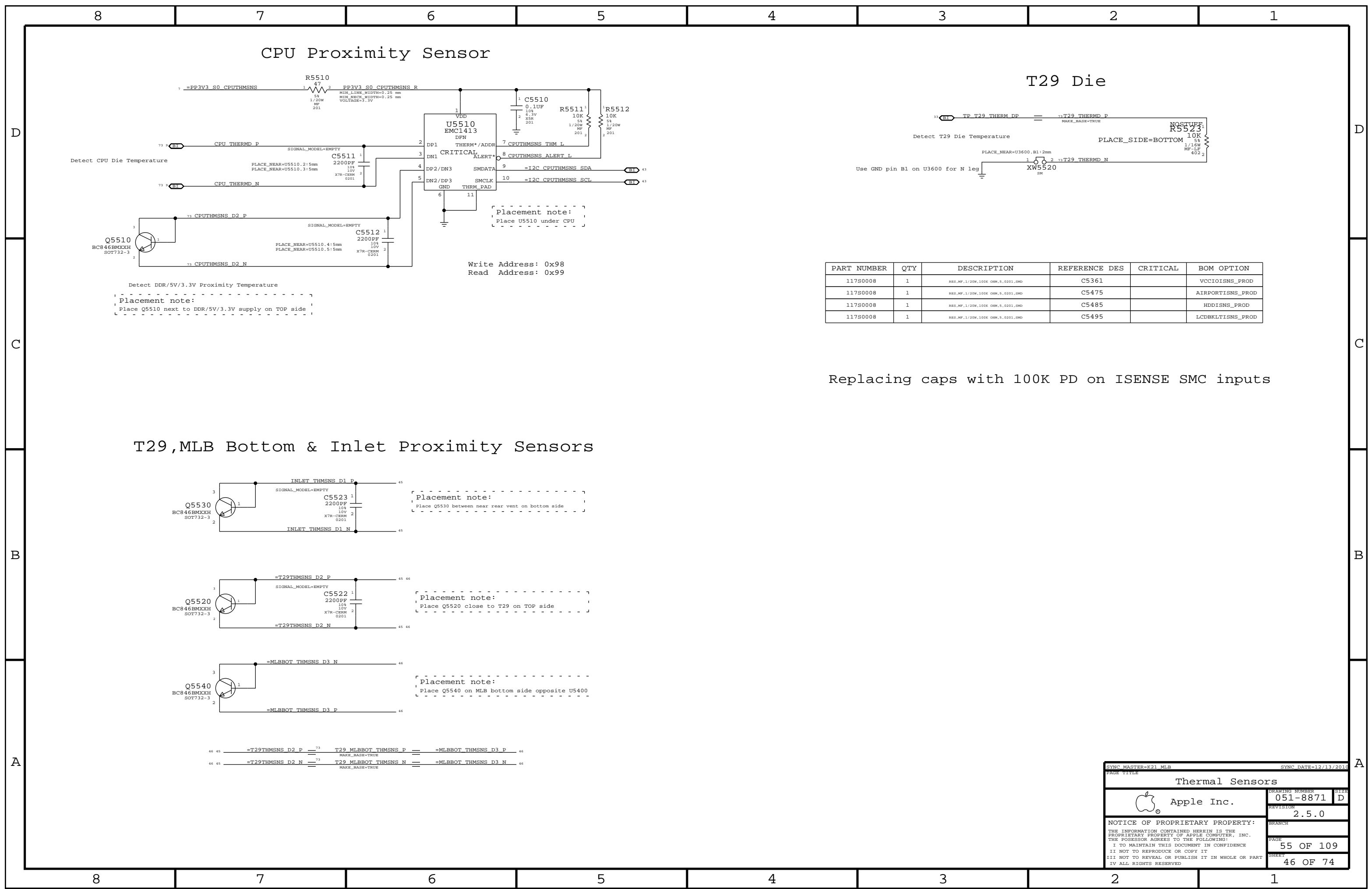
117S0008

1

RES,MF,1/20W,100K OHM,5,0201,SMD

C5495

LCDCLKTISNS_PROD



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Description

Reference Des

Critical

BOM Option

117S0008

1

RES,MF,1/20W,100K OHM,S,0201,SMD

C5361

VCCIOISNS_PROD

117S0008

1

RES,MF,1/20W,100K OHM,S,0201,SMD

C5475

AIRPORTISNS_PROD

117S0008

1

RES,MF,1/20W,100K OHM,S,0201,SMD

C5485

HDDISNS_PROD

117S0008

1

RES,MF,1/20W,100K OHM,S,0201,SMD

C5495

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Critical

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117S0008

1

RES,MF,1/20W,100K OHM,S,0201,SMD

C5361

VCCIOISNS_PROD

117S0008

1

RES,MF,1/20W,100K OHM,S,0201,SMD

C5475

AIRPORTISNS_PROD

117S0008

1

RES,MF,1/20W,100K OHM,S,0201,SMD

C5485

HDDISNS_PROD

117S0008

1

RES,MF,1/20W,100K OHM,S,0201,SMD

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Part Number

Qty

Description

Reference Des

Critical

BOM Option

117S0008

1

RES,MF,1/20W,100K OHM,5,0201,SMD

C5361

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117S0008

1

RES,MF,1/20W,100K OHM,5,0201,SMD

C5475

AIRPORTISNS_PROD

117S0008

1

RES,MF,1/20W,100K OHM,5,0201,SMD

C5485

HDDISNS_PROD

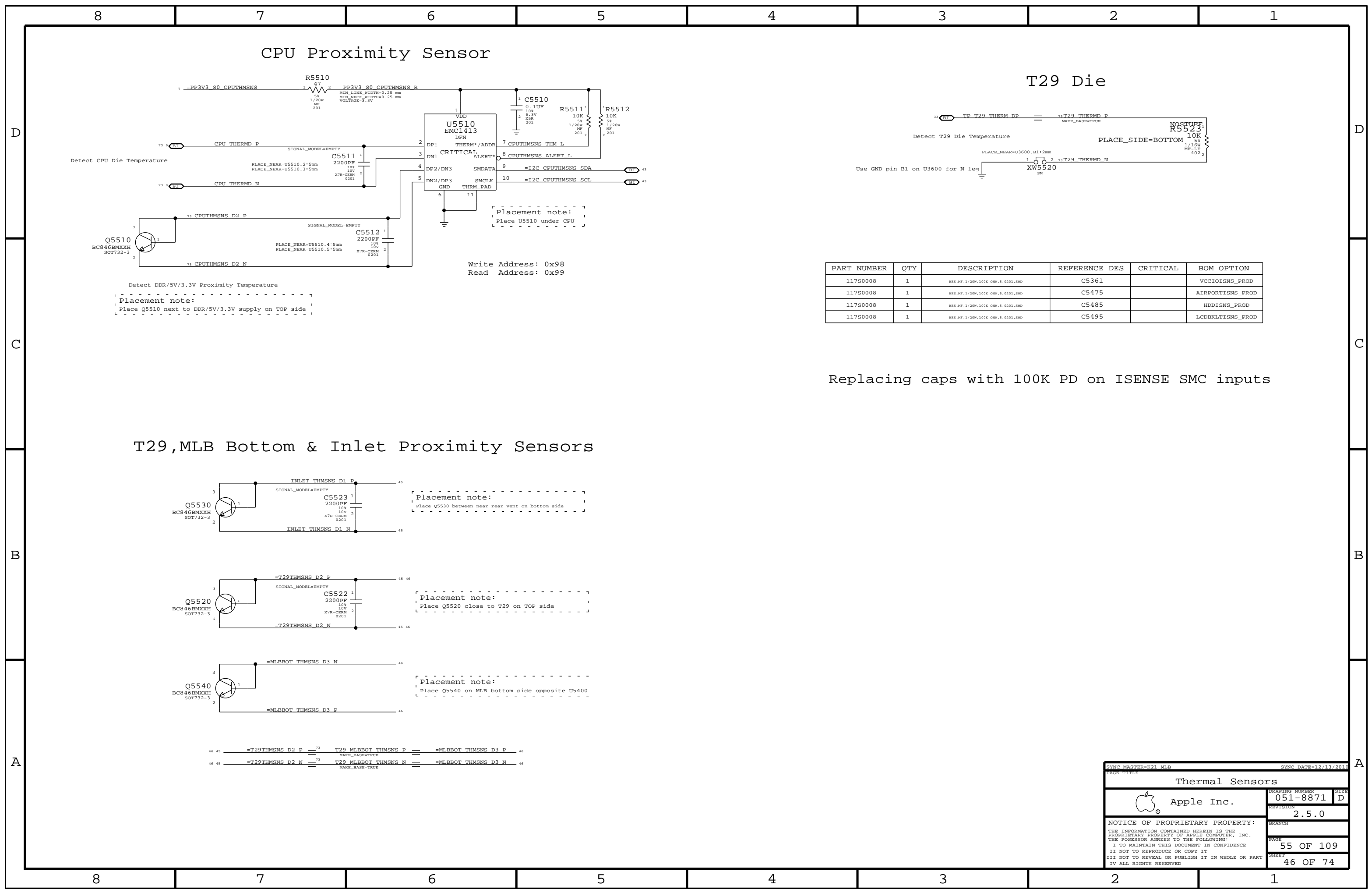
117S0008

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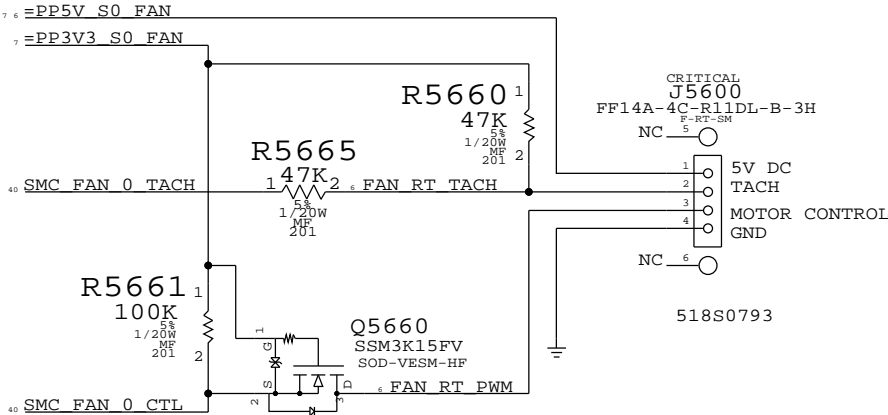
RES,MF,1/20W,100K OHM,5,0201,SMD

C5495

LCDCLKTISNS_PROD

[illegible]

FAN CONNECTOR



D

C

B

A

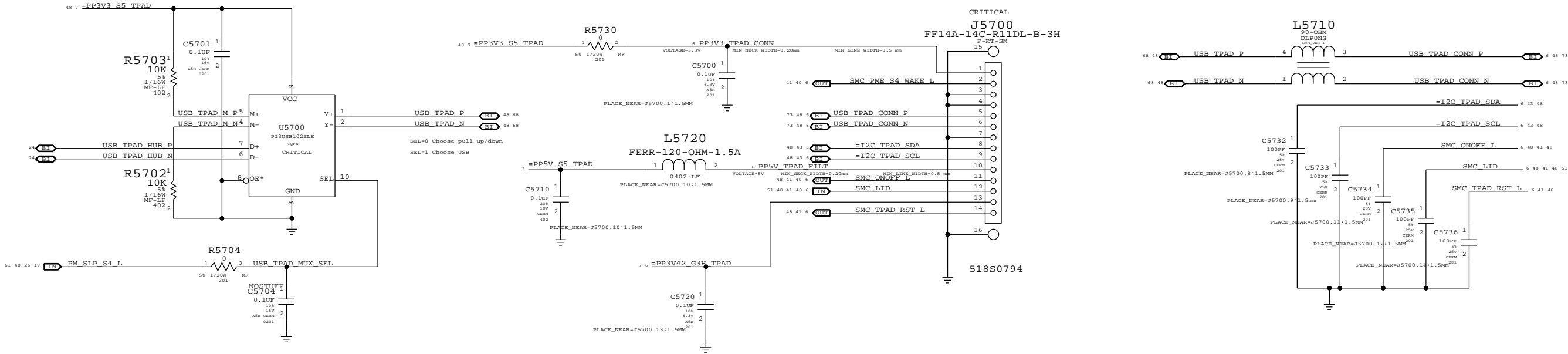
D

C

B

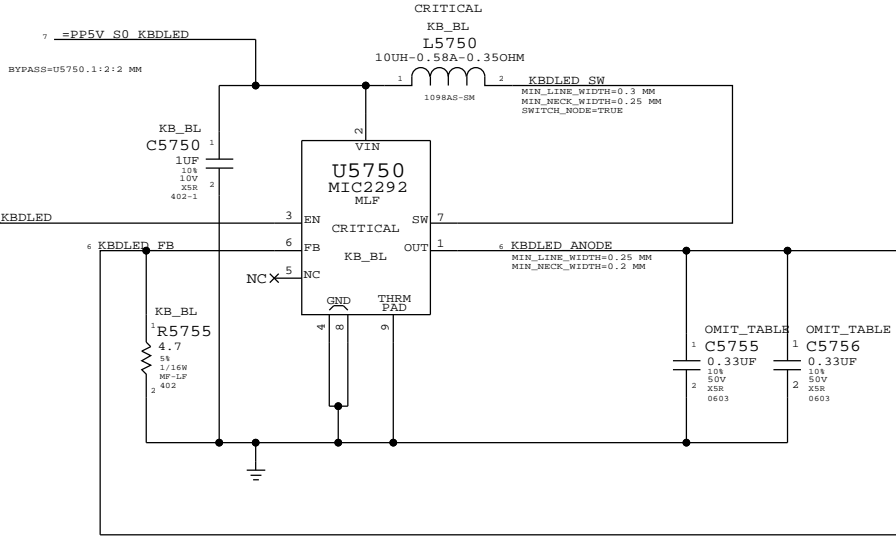
A

IPD Flex Connector

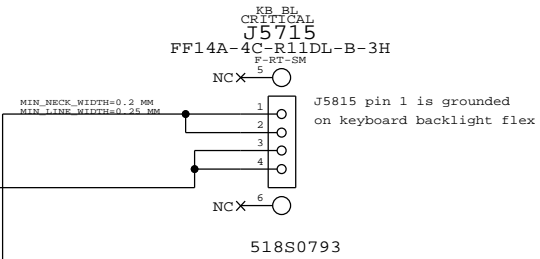


Keyboard Backlight Driver & Detection


To detect Keyboard backlight, SMC will tristate and read SMC_SYS_KBDLED:
If LOW, keyboard backlight present
If HIGH, keyboard backlight not present
R5853 always stuffed, R5854 only grounded when KB BL flex connected.

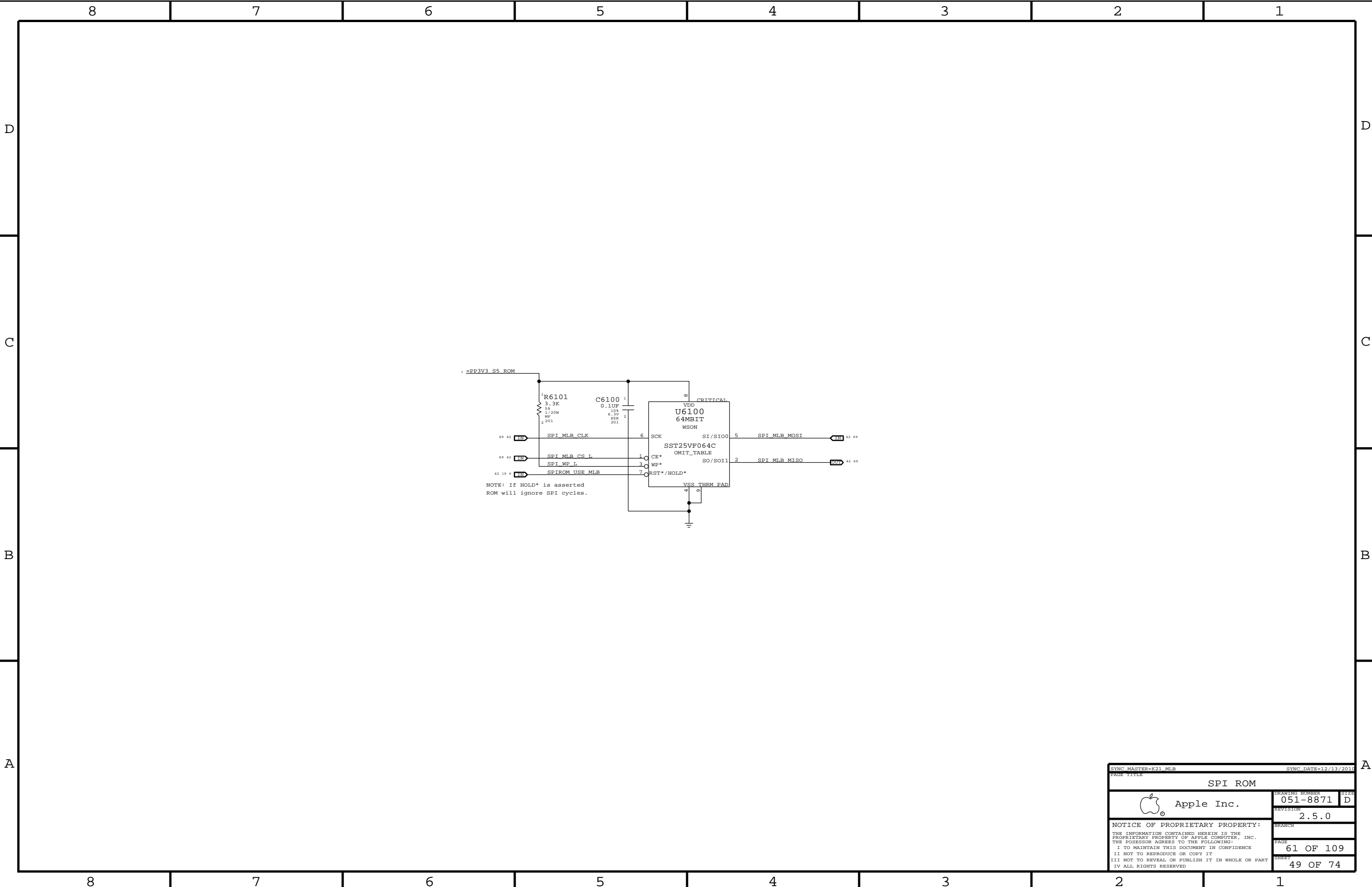


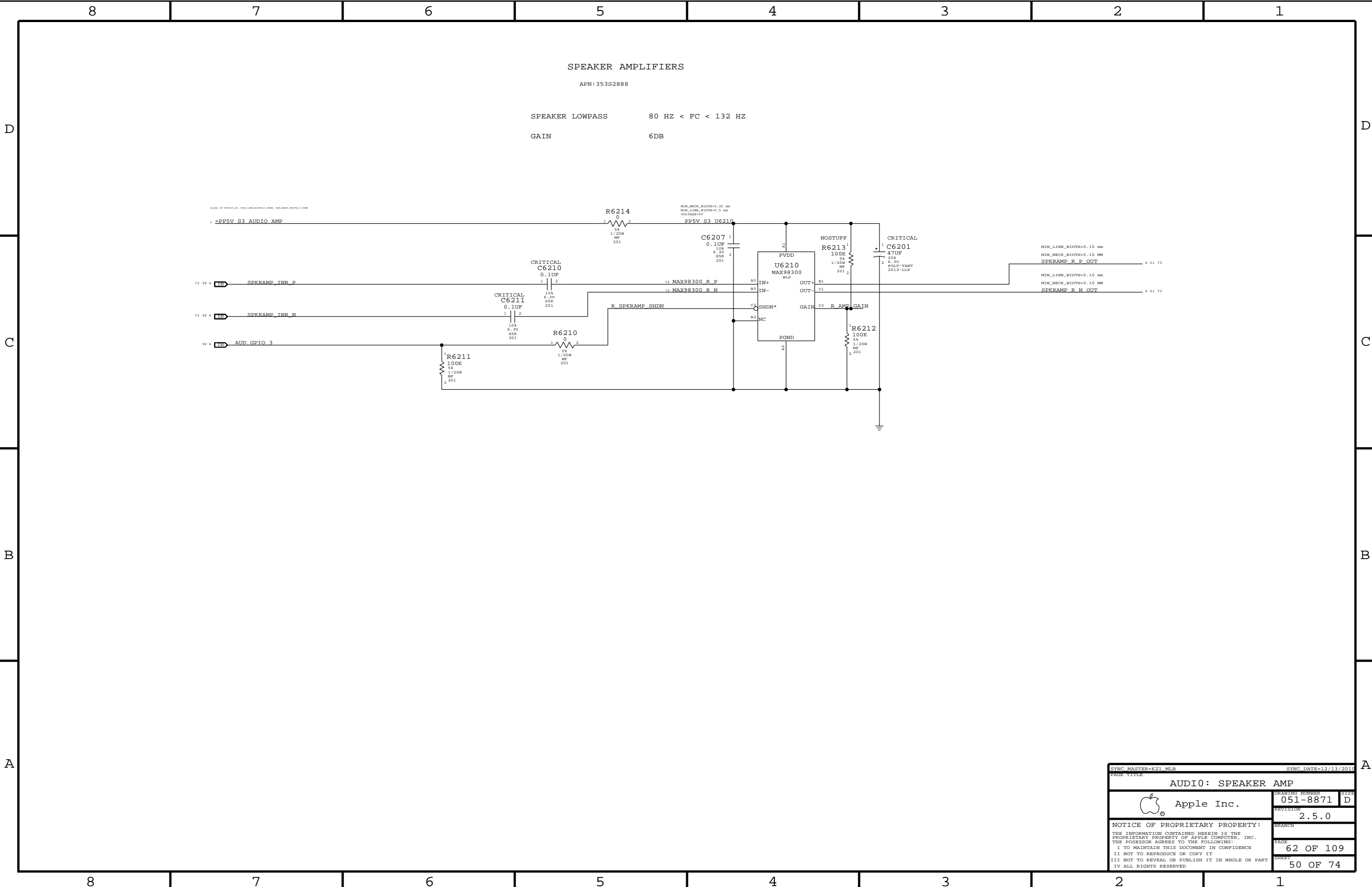
Keyboard Backlight Connector

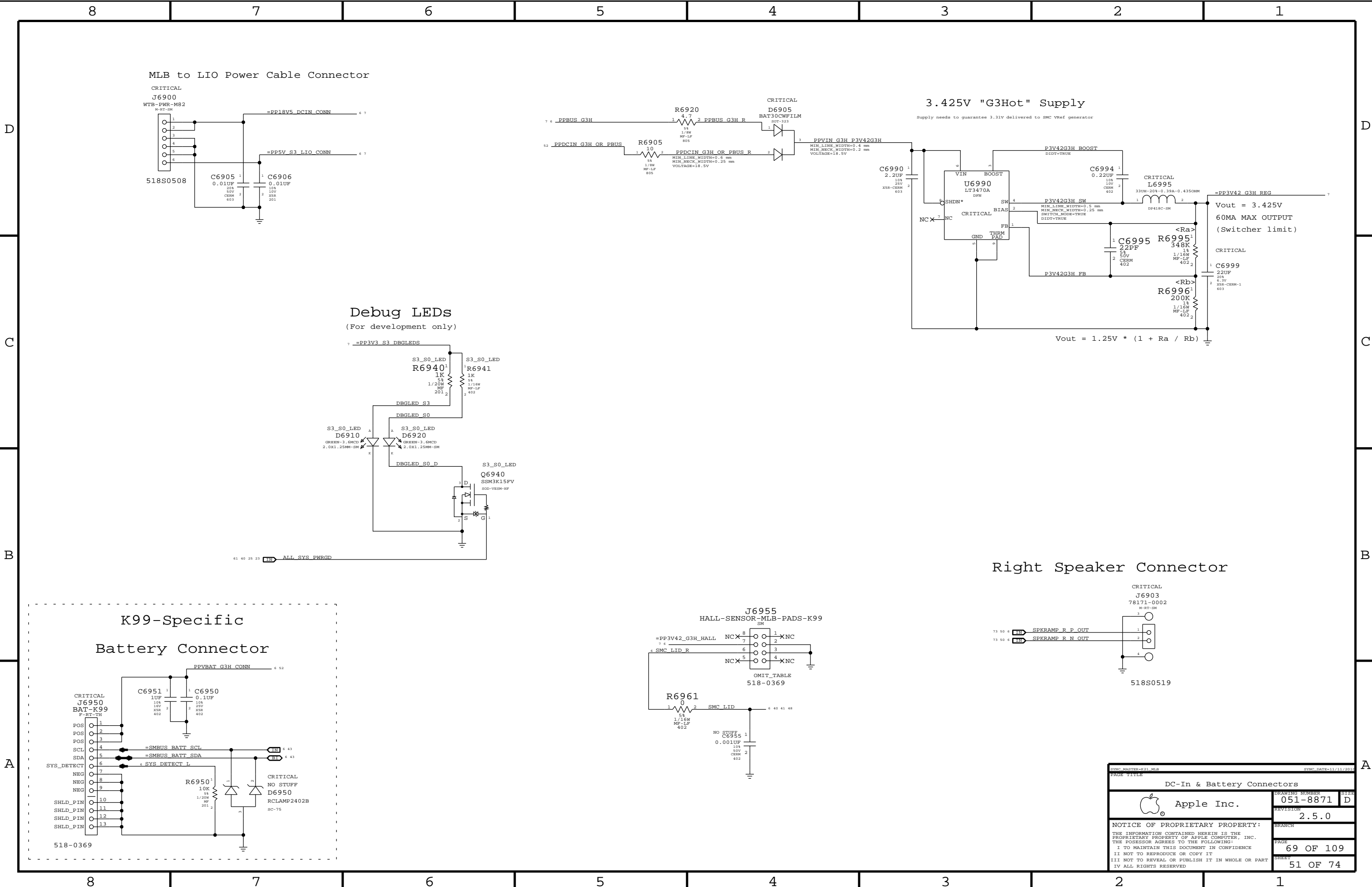


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0704	2	CAP, CER, 0.22UF, 10V, 50V, X5R, 0603	C5756, C5755		KB_BL

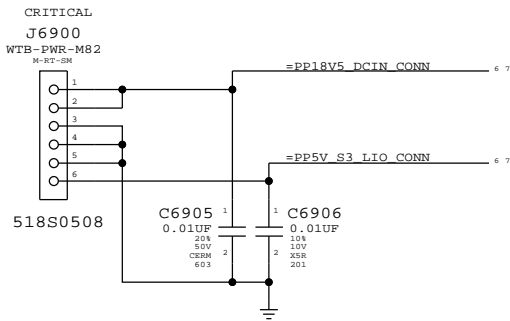
SYNC MASTER=K21 MLB		SYNC DATE=12/13/2010	
PAGE TITLE			
IPD / KBD Backlight			
	Apple Inc.	DRAWING NUMBER	051-8871
		SIZE	D
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		PAGE	57 OF 109
		SHEET	48 OF 74



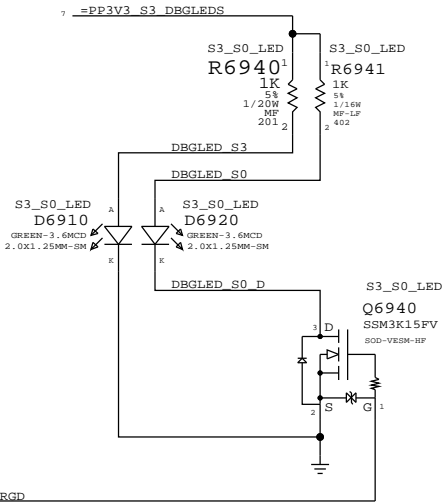




MLB to LIO Power Cable Connector

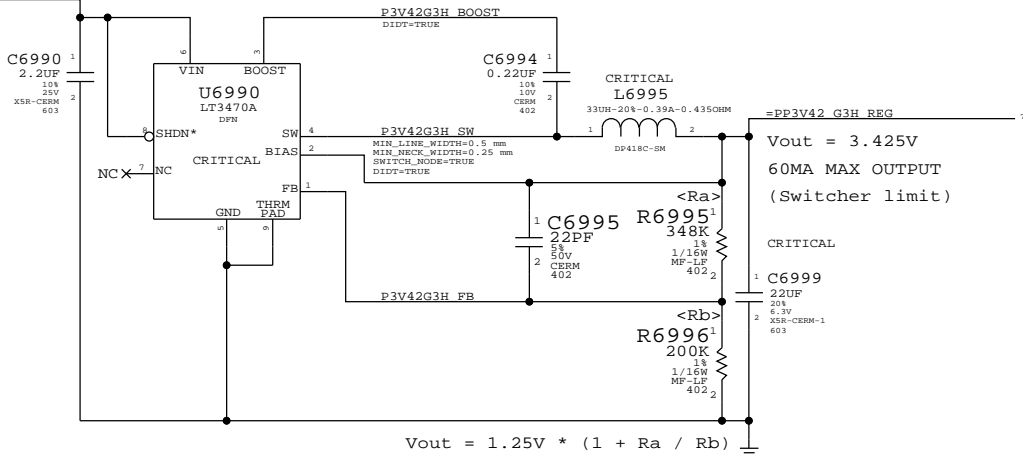


Debug LEDs
(For development only)

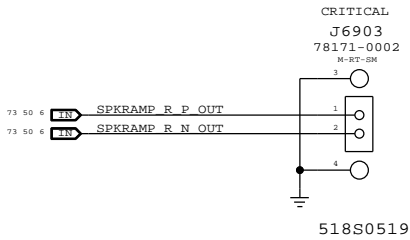


3.425V "G3Hot" Supply

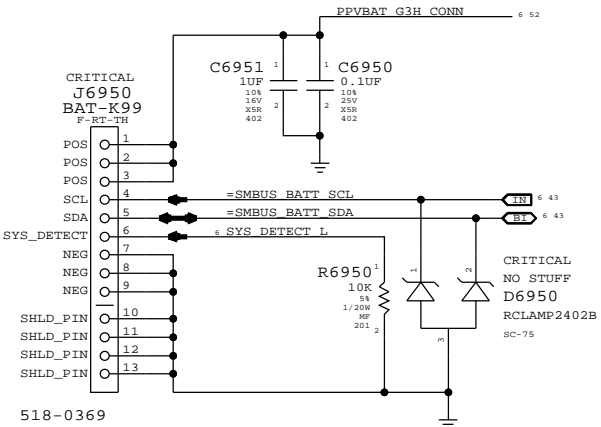
Supply needs to guarantee 3.31V delivered to SMC VRef generator



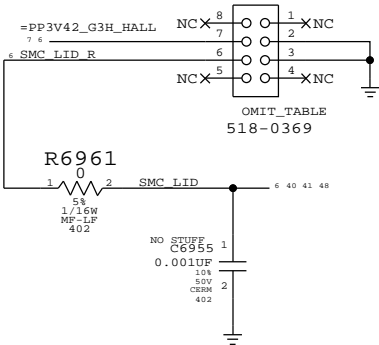
Right Speaker Connector




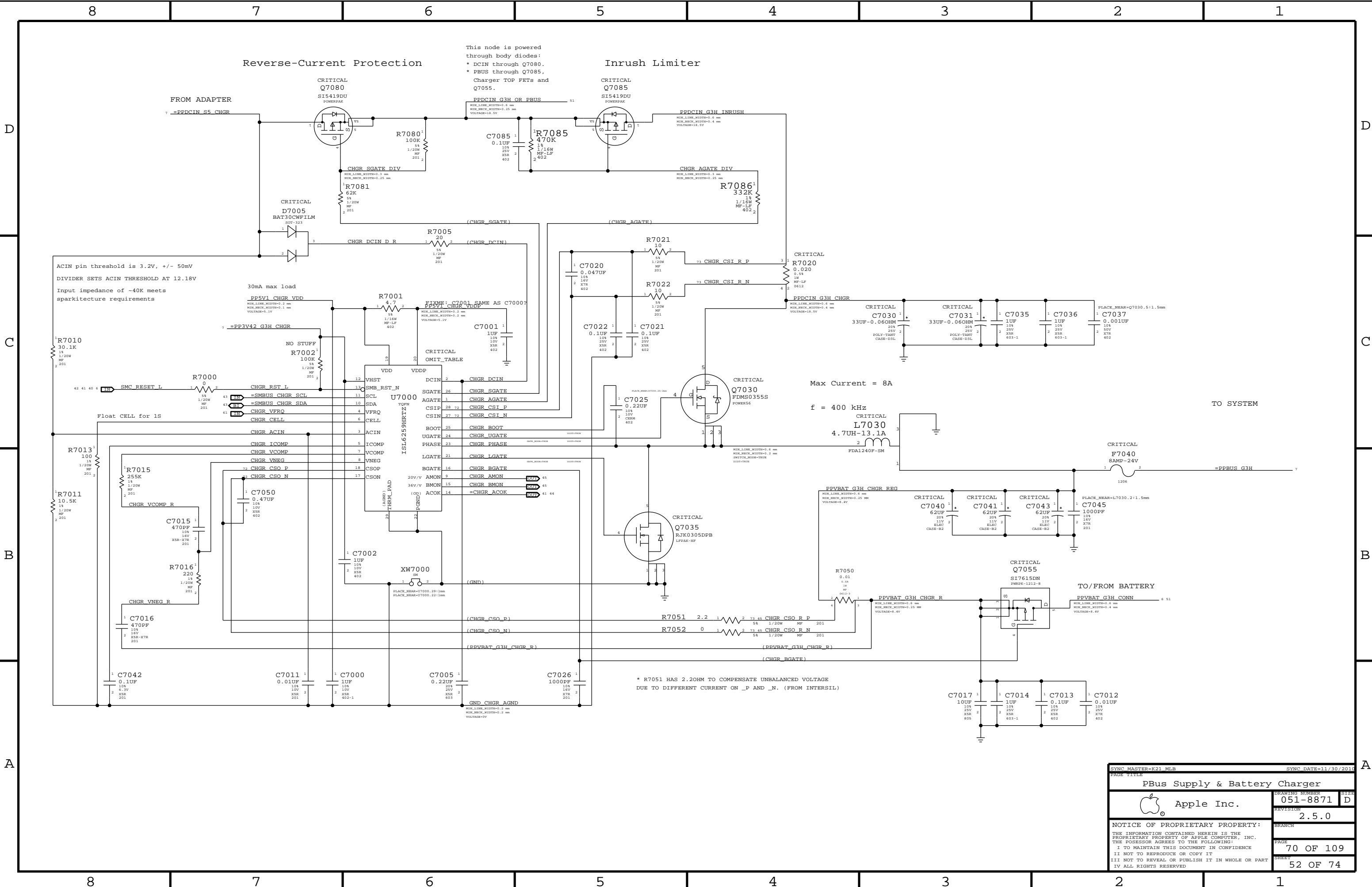
K99-Specific
Battery Connector

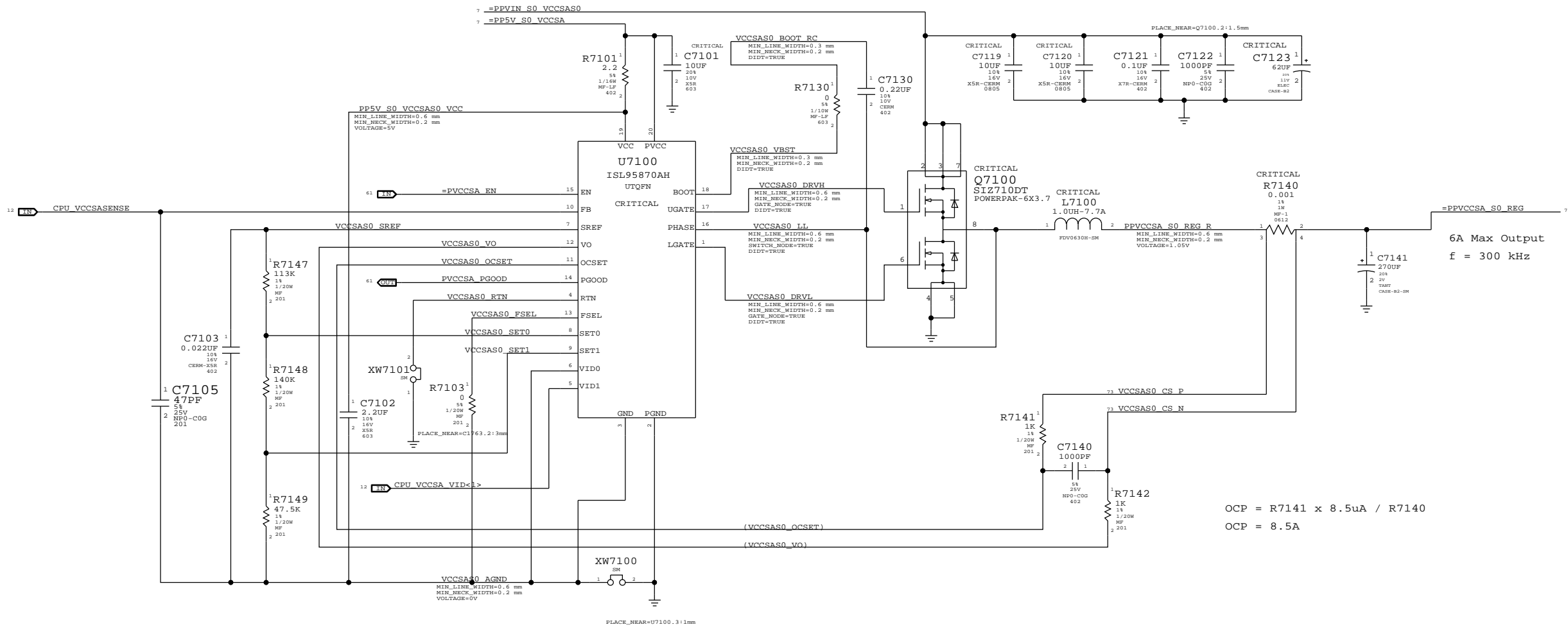


J6955
HALL-SENSOR-MLB-PADS-K99



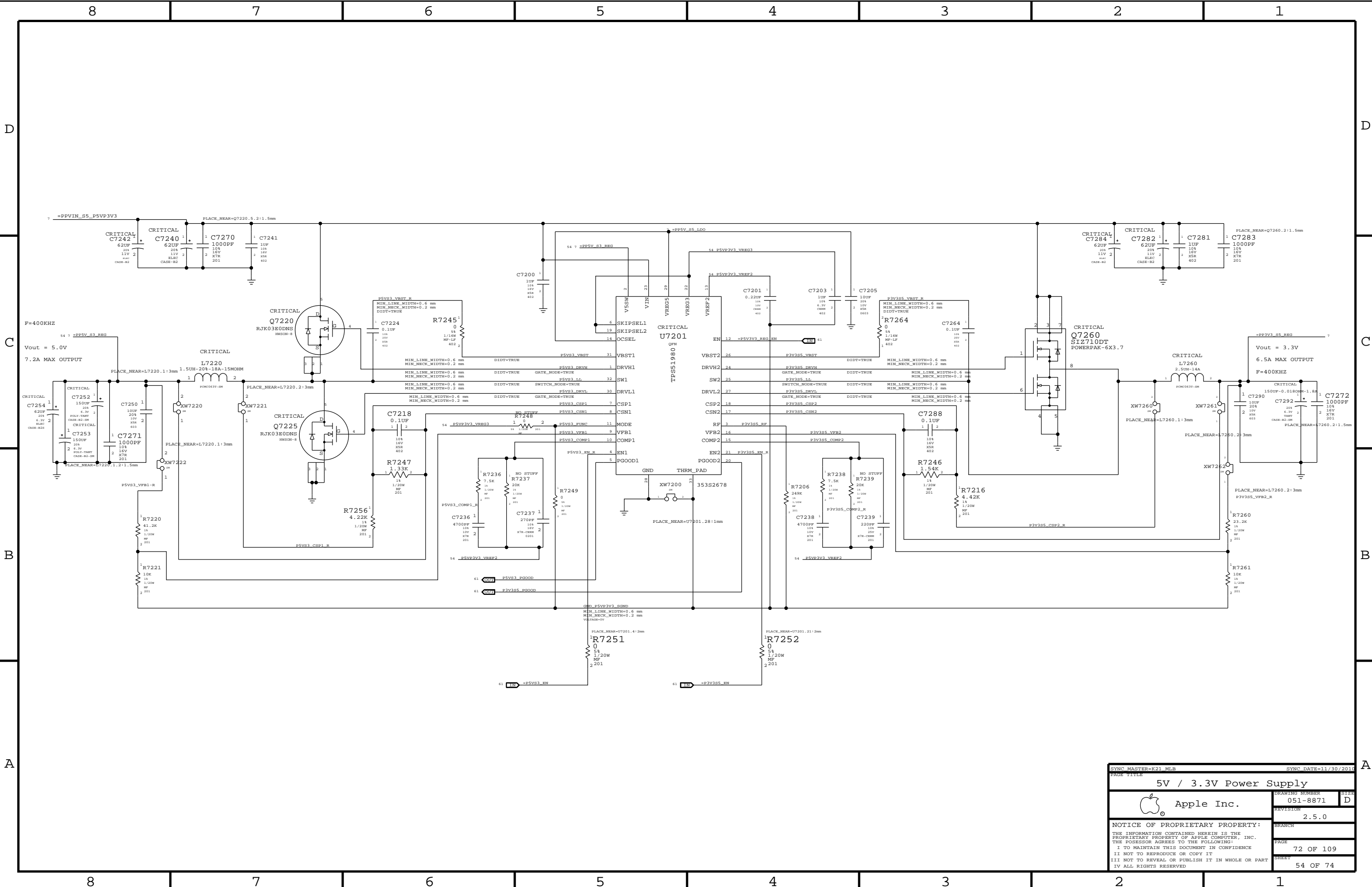
SYMC PARTSHEET:MLB-M82		SYMC DATE:11/11/2011	
PAGE TITLE			
DC-In & Battery Connectors			
 Apple Inc.		DRAWING NUMBER	051-8871
		REVISION	2.5.0
		BRANCH	
		PAGE	69 OF 109
		SHEET	51 OF 74
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VID1	VID0	Voltage
0	0	0.9V
1	0	0.8V

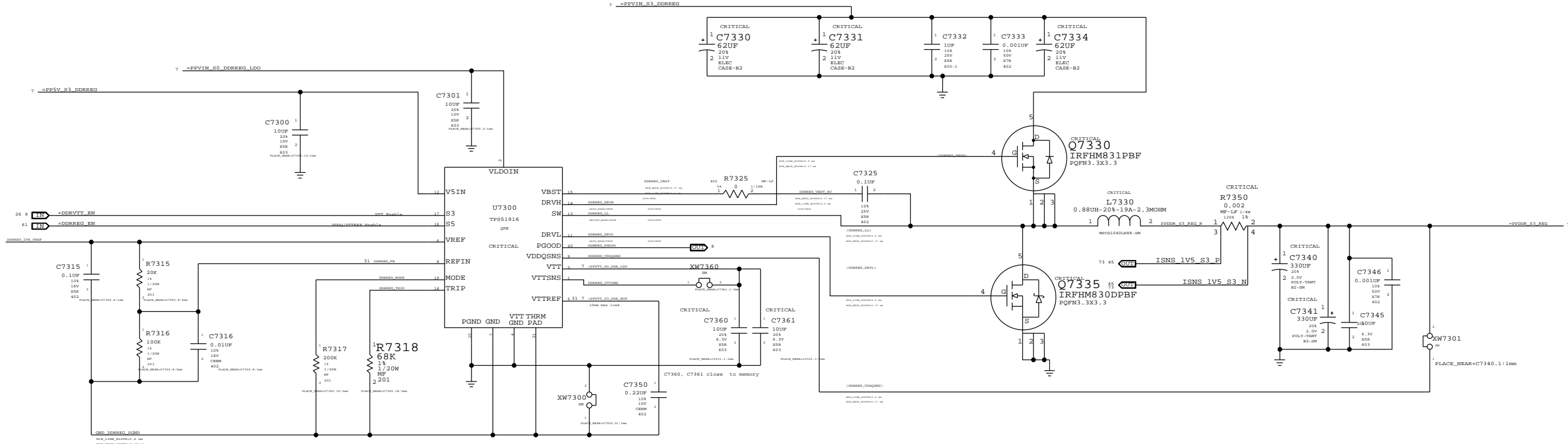
$$OCP = R7141 \times 8.5\mu A / R7140$$
$$OCP = 8.5A$$




D
C
B
A

D
C
B
A

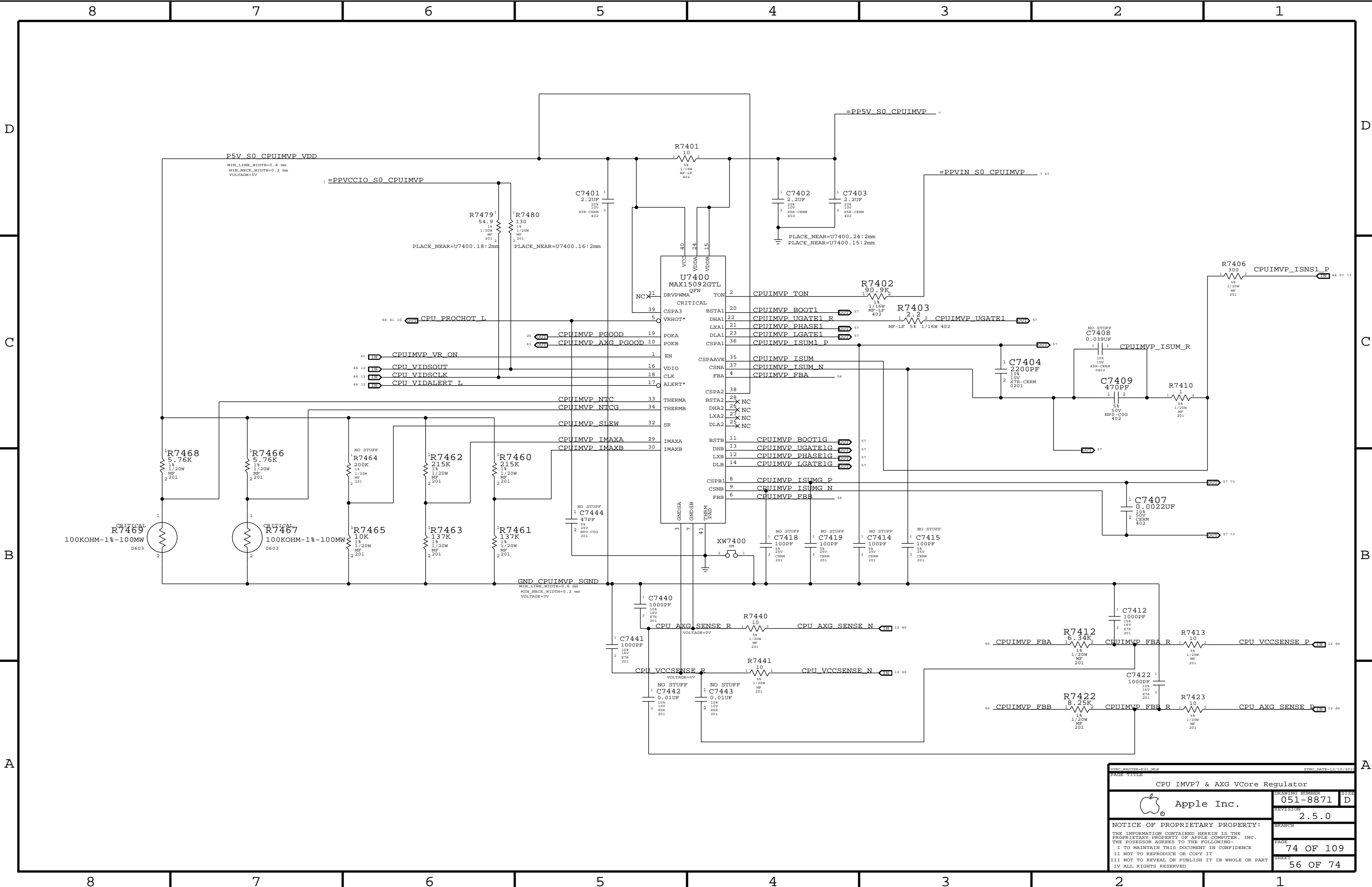
8 7 6 5 4 3 2 1



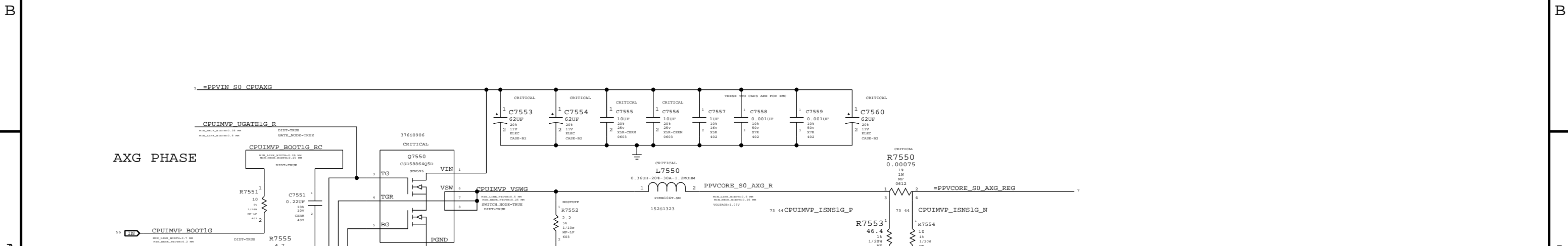
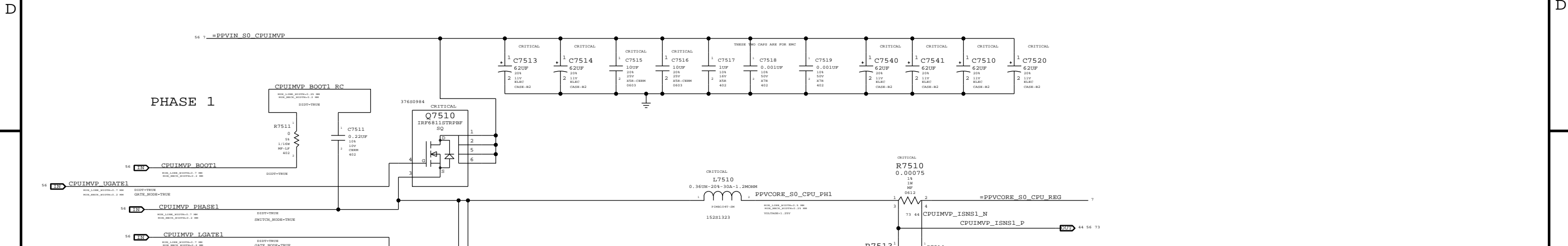
Vout = 1.5V
14.1A max output
(Q7335 limit)
f = 400 kHz

PAGE TITLE			
1.5V DDR3 Supply			
 Apple Inc.	DRAWING NUMBER	051-8871	SIZE D
	REVISION	2.5.0	
	BRANCH		
	PAGE	73 OF 109	
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SHEET 55 OF 74			

8 7 6 5 4 3 2 1



8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---



The image displays a multi-page schematic diagram of a CPU board, specifically showing pages 1 through 8. The diagram includes various components like resistors, capacitors, and integrated circuits, along with their electrical specifications and connections. A title block on the right side of page 1 provides drawing information.

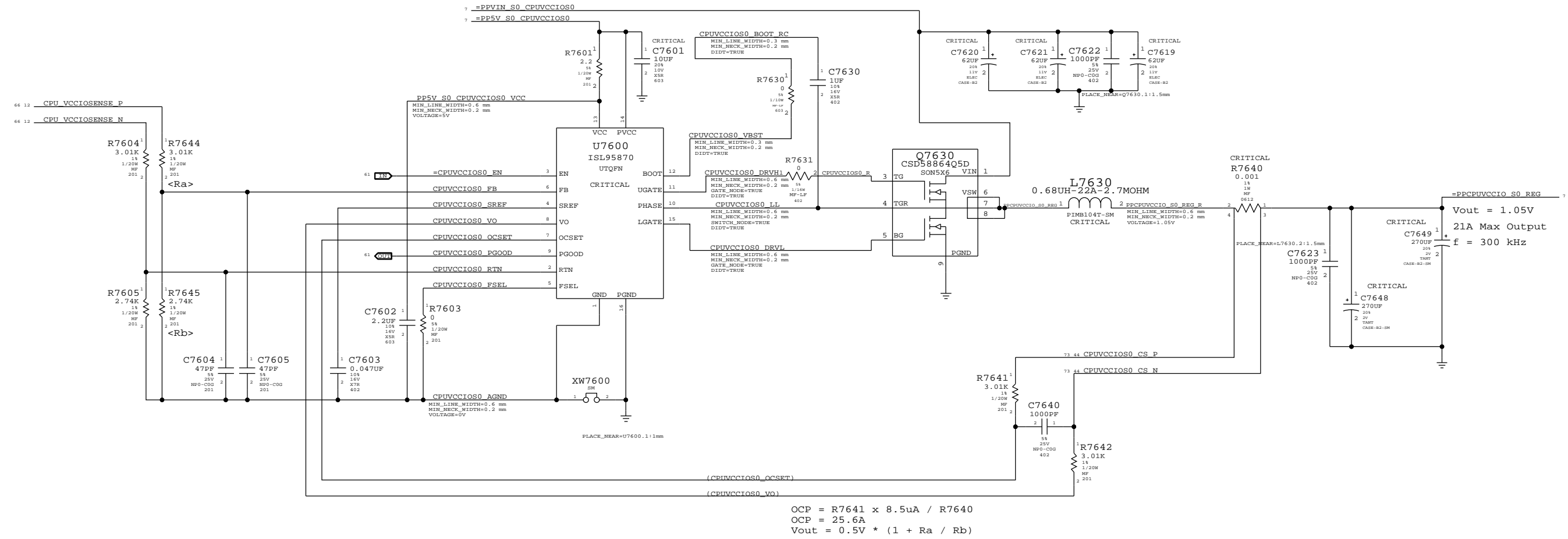
Page 1 Title Block:

DRAWN: 12/11/11	
PAGE TITLE	
CPU IMV7 & AXG VCore Output	
DRAWING NUMBER	051-8871
REVISION	2.5.0
BRANCH	
PAGE	75 OF 109
SHEET	57 OF 74

Page 1 Schematic Details:

- Component C7552:** 0.001UF, 10V, 50V, CPM6, 402.
- Component C7574:** 1000PF, 10V, 16V, 37R, 201.
- Component C7575:** 10V, 16V, 37R, 201.
- Component C7576:** 10V, 16V, 37R, 201.
- Component C7577:** 10V, 16V, 37R, 201.
- Component C7578:** 10V, 16V, 37R, 201.
- Component C7579:** 10V, 16V, 37R, 201.
- Component C7580:** 10V, 16V, 37R, 201.
- Component C7581:** 10V, 16V, 37R, 201.
- Component C7582:** 10V, 16V, 37R, 201.
- Component C7583:** 10V, 16V, 37R, 201.
- Component C7584:** 10V, 16V, 37R, 201.
- Component C7585:** 10V, 16V, 37R, 201.
- Component C7586:** 10V, 16V, 37R, 201.
- Component C7587:** 10V, 16V, 37R, 201.
- Component C7588:** 10V, 16V, 37R, 201.
- Component C7589:** 10V, 16V, 37R, 201.
- Component C7590:** 10V, 16V, 37R, 201.
- Component C7591:** 10V, 16V, 37R, 201.
- Component C7592:** 10V, 16V, 37R, 201.
- Component C7593:** 10V, 16V, 37R, 201.
- Component C7594:** 10V, 16V, 37R, 201.
- Component C7595:** 10V, 16V, 37R, 201.
- Component C7596:** 10V, 16V, 37R, 201.
- Component C7597:** 10V, 16V, 37R, 201.
- Component C7598:** 10V, 16V, 37R, 201.
- Component C7599:** 10V, 16V, 37R, 201.
- Component C7600:** 10V, 16V, 37R, 201.
- Component C7601:** 10V, 16V, 37R, 201.
- Component C7602:** 10V, 16V, 37R, 201.
- Component C7603:** 10V, 16V, 37R, 201.
- Component C7604:** 10V, 16V, 37R, 201.
- Component C7605:** 10V, 16V, 37R, 201.
- Component C7606:** 10V, 16V, 37R, 201.
- Component C7607:** 10V, 16V, 37R, 201.
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- Component C7609:** 10V, 16V, 37R, 201.
- Component C7610:** 10V, 16V, 37R, 201.
- Component C7611:** 10V, 16V, 37R, 201.
- Component C7612:** 10V, 16V, 37R, 201.
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- Component C7615:** 10V, 16V, 37R, 201.
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- Component C7619:** 10V, 16V, 37R, 201.
- Component C7620:** 10V, 16V, 37R, 201.
- Component C7621:** 10V, 16V, 37R, 201.
- Component C7622:** 10V, 16V, 37R, 201.
- Component C7623:** 10V, 16V, 37R, 201.
- Component C7624:** 10V, 16V, 37R, 201.
- Component C7625:** 10V, 16V, 37R, 201.
- Component C7626:** 10V, 16V, 37R, 201.
- Component C7627:** 10V, 16V, 37R, 201.
- Component C7628:** 10V, 16V, 37R, 201.
- Component C7629:** 10V, 16V, 37R, 201.
- Component C7630:** 10V, 16V, 37R, 201.
- Component C7631:** 10V, 16V, 37R, 201.
- Component C7632:** 10V, 16V, 37R, 201.
- Component C7633:** 10V, 16V, 37R, 201.
- Component C7634:** 10V, 16V, 37R, 201.
- Component C7635:** 10V, 16V, 37R, 201.
- Component C7636:** 10V, 16V, 37R, 201.
- Component C7637:** 10V, 16V, 37R, 201.
- Component C7638:** 10V, 16V, 37R, 201.
- Component C7639:** 10V, 16V, 37R, 201.
- Component C7640:** 10V, 16V, 37R, 201.
- Component C7641:** 10V, 16V, 37R, 201.
- Component C7642:** 10V, 16V, 37R, 201.
- Component C7643:** 10V, 16V, 37R, 201.
- Component C7644:** 10V, 16V, 37R, 201.
- Component C7645:** 10V, 16V, 37R, 201.
- Component C7646:** 10V, 16V, 37R, 201.
- Component C7647:** 10V, 16V, 37R, 201.
- Component C7648:** 10V, 16V, 37R, 201.
- Component C7649:** 10V, 16V, 37R, 201.
- Component C7650:** 10V, 16V, 37R, 201.
- Component C7651:** 10V, 16V, 37R, 201.
- Component C7652:** 10V, 16V, 37R, 201.
- Component C7653:** 10V, 16V, 37R, 201.
- Component C7654:** 10V, 16V, 37R, 201.
- Component C7655:** 10V, 16V, 37R, 201.
- Component C7656:** 10V, 16V, 37R, 201.
- Component C7657:** 10V, 16V, 37R, 201.
- Component C7658:** 10V, 16V, 37R, 201.
- Component C7659:** 10V, 16V, 37R, 201.
- Component C7660:** 10V, 16V, 37R, 201.
- Component C7661:** 10V, 16V, 37R, 201.
- Component C7662:** 10V, 16V, 37R, 201.
- Component C7663:** 10V, 16V, 37R, 201.
- Component C7664:** 10V, 16V, 37R, 201.
- Component C7665:** 10V, 16V, 37R, 201.
- Component C7666:** 10V, 16V, 37R, 201.
- Component C7667:** 10V, 16V, 37R, 201.
- Component C7668:** 10V, 16V, 37R, 201.
- Component C7669:** 10V, 16V, 37R, 201.
- Component C7670:** 10V, 16V, 37R, 201.
- Component C7671:** 10V, 16V, 37R, 201.
- Component C7672:** 10V, 16V, 37R, 201.
- Component C7673:** 10V, 16V, 37R, 201.
- Component C7674:** 10V, 16V, 37R, 201.
- Component C7675:** 10V, 16V, 37R, 201.

CPU VCCIO (1.05V S0) Regulator



D

C

B

A

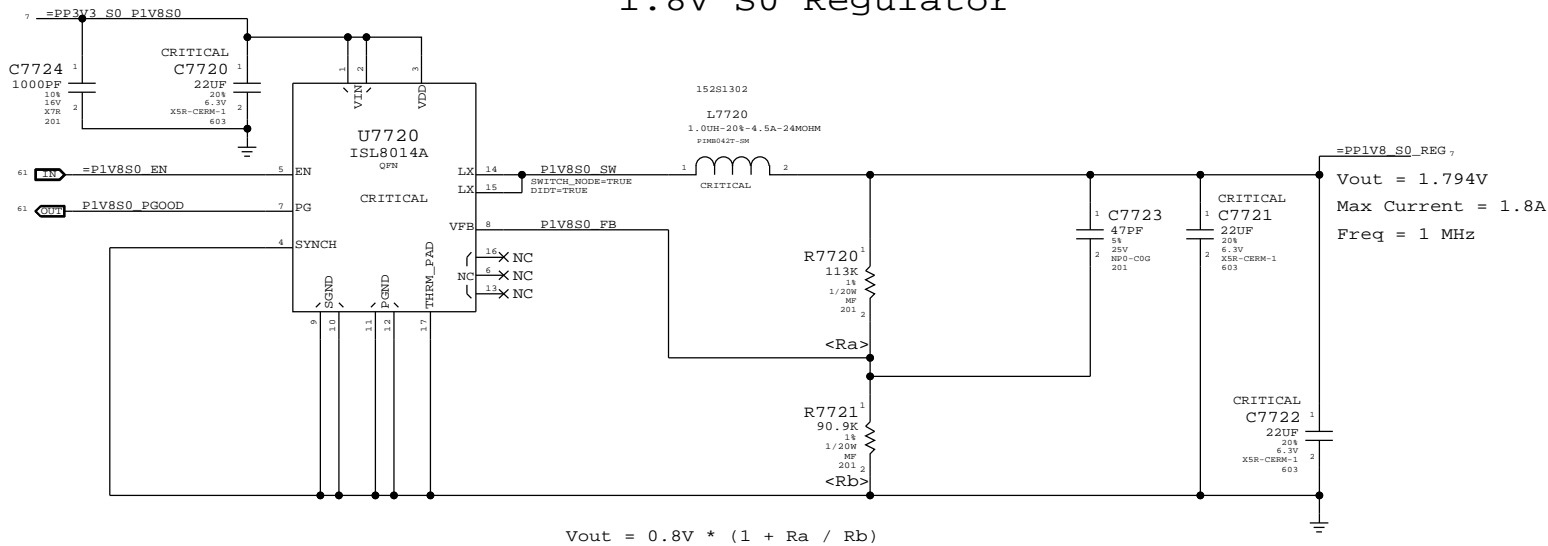
D

C

B

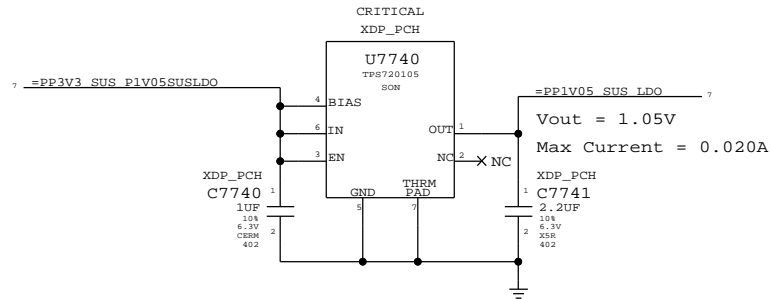
A

1.8V S0 Regulator

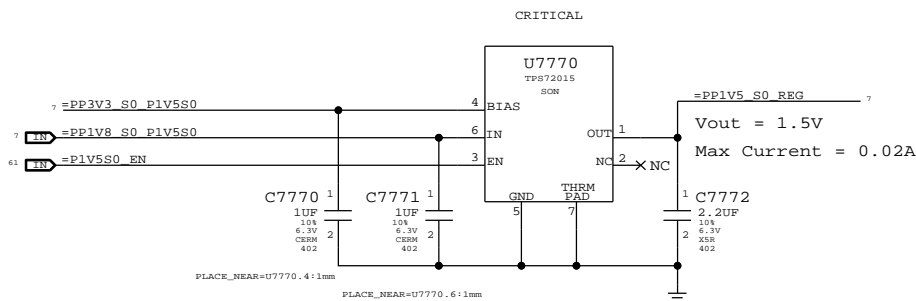


1.05V SUS LDO

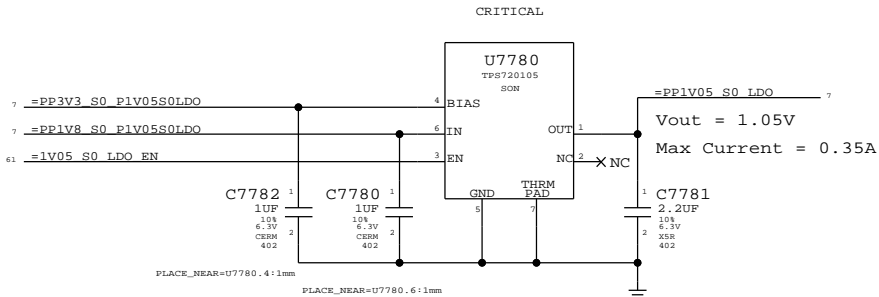
Cougar Point requires JTAG pull-ups to be powered at 1.05V when SUS suspend well is active. Pull-ups (3) must be 51 ohms to support XDP (not required in production). 70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.




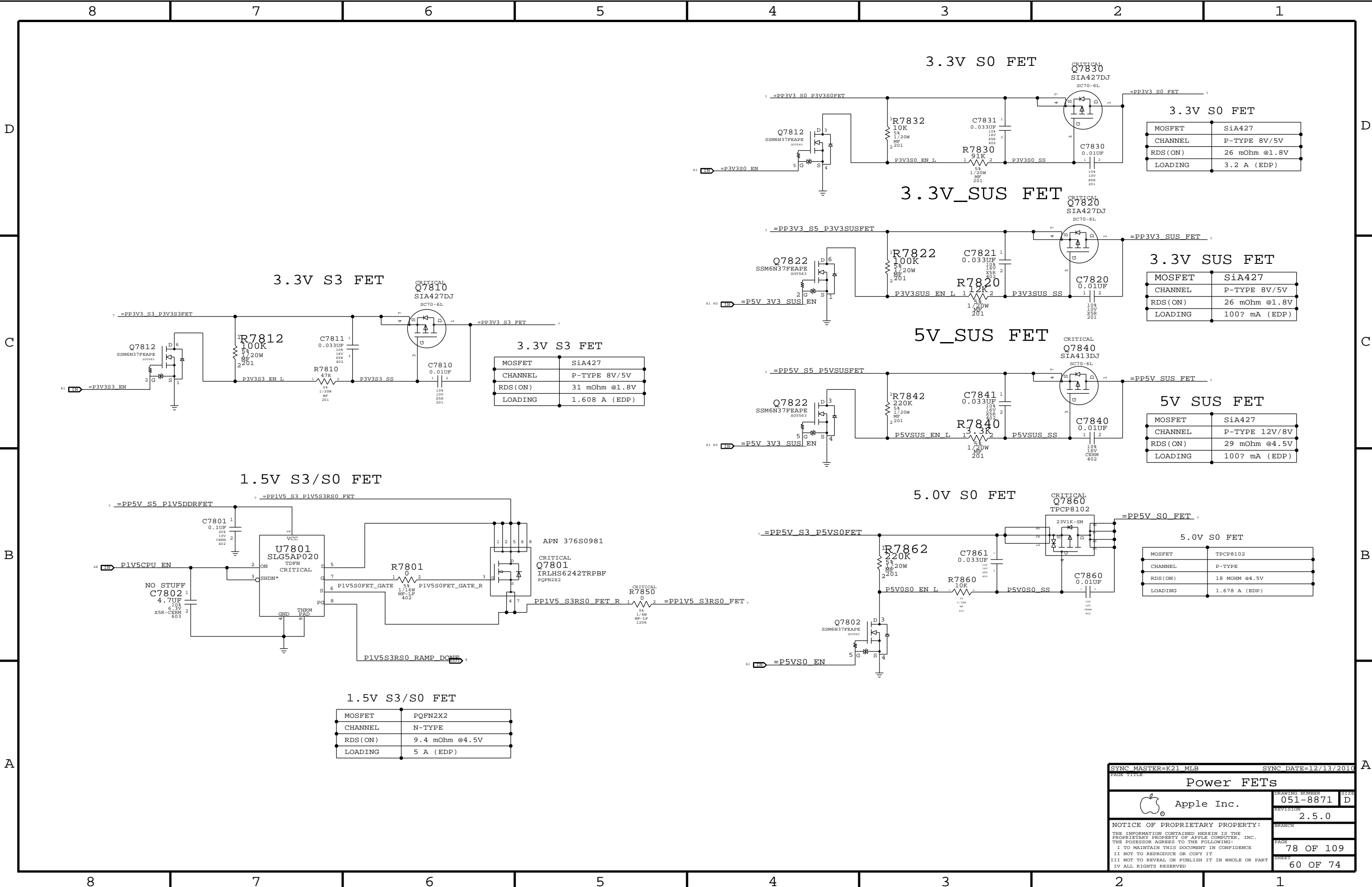
1.5V S0 LDO

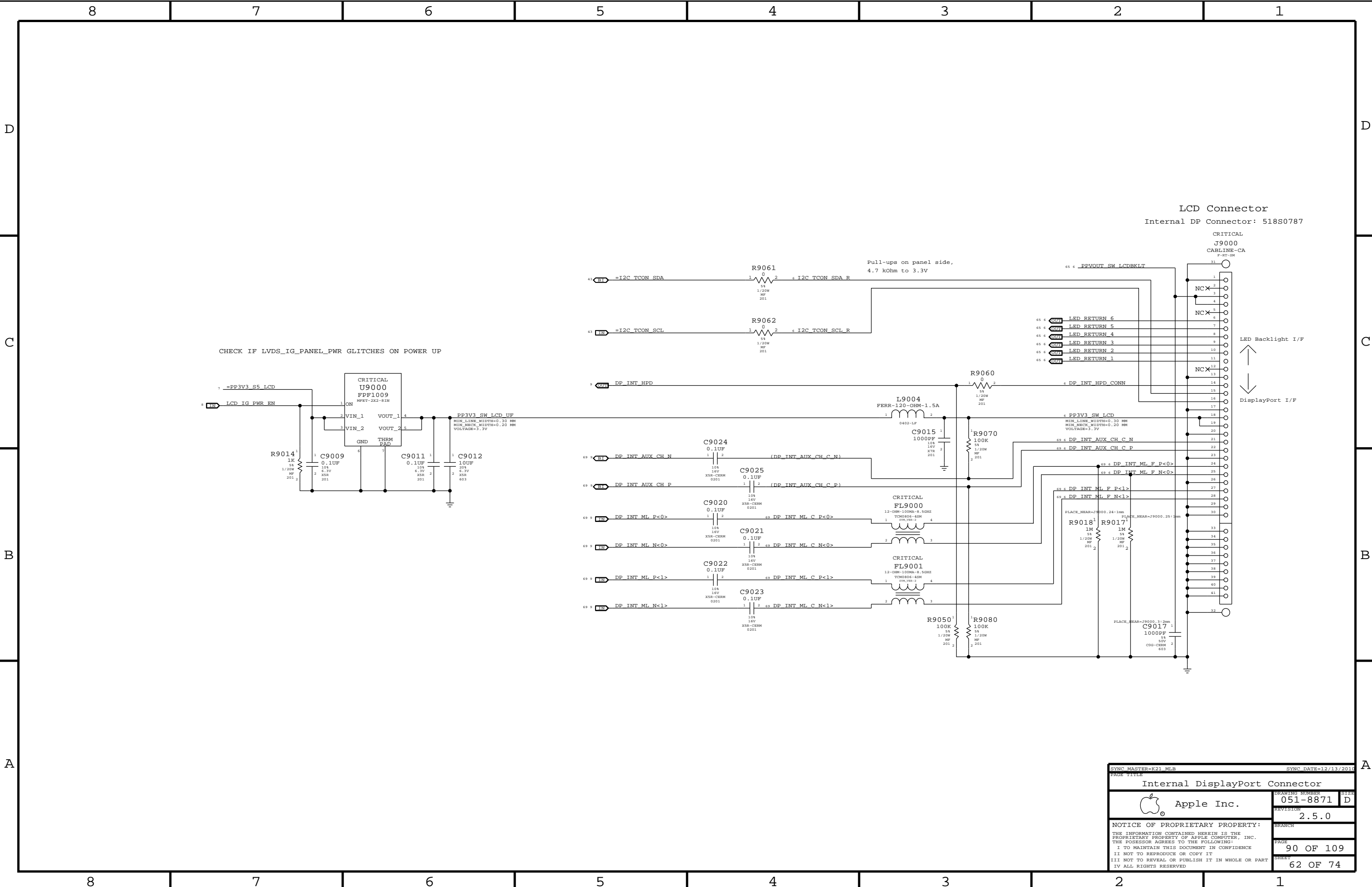


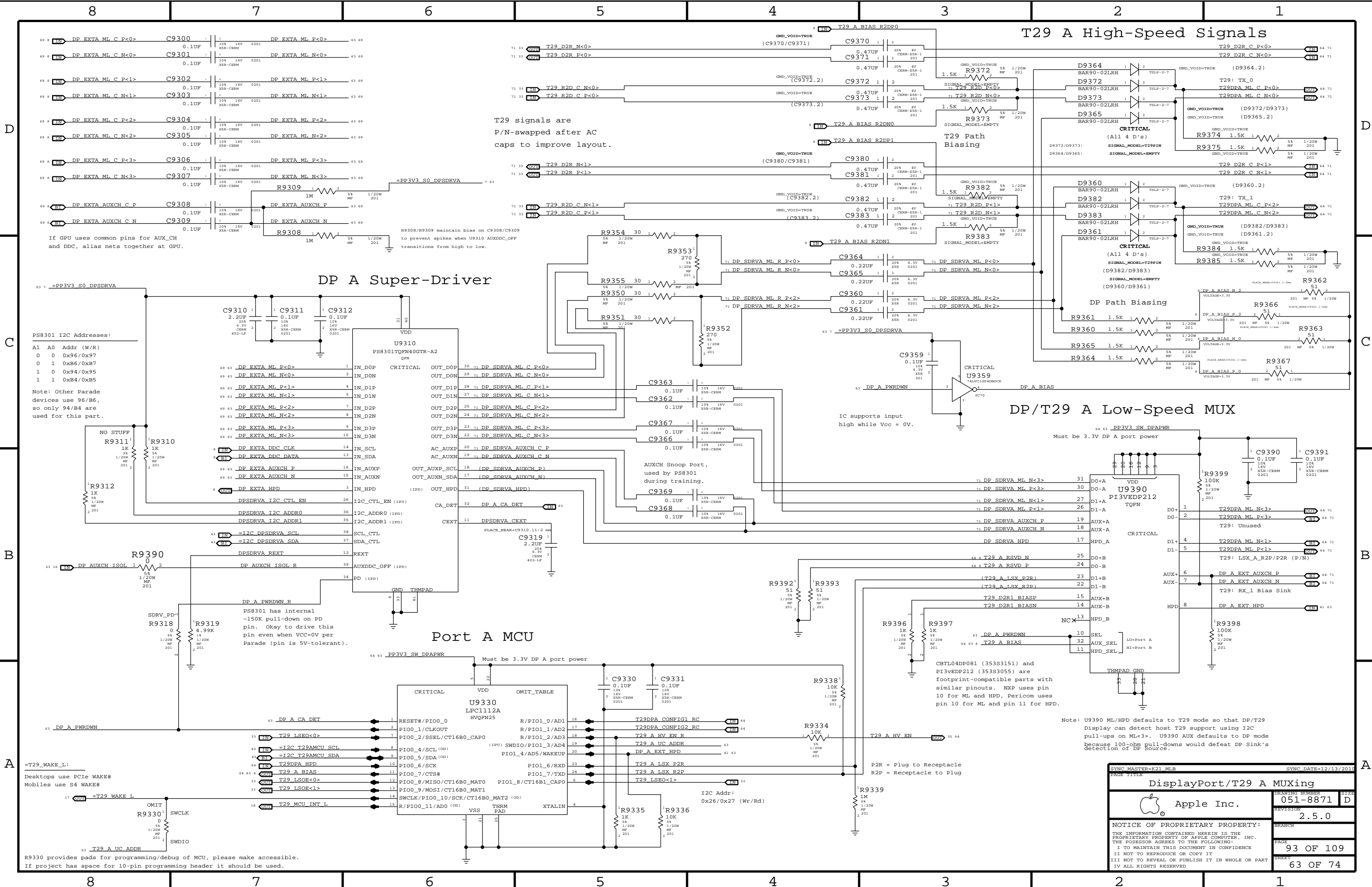
1.05V S0 LDO



SYNC MASTER=K21 MLB		SYNC DATE=12/13/2010	
PAGE TITLE			
Misc Power Supplies			
	Apple Inc.	DRAWING NUMBER	051-8871
		REVISION	2.5.0
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R9308/R9309 maintain bias on C9308/C9309 to prevent spikes when U9310 AUXDDC_OFF transitions from high to low.

PS8301 I2C Addresses:

A1 A0 Addr (W/R)
0 0 0x96/0x97
0 1 0xB6/0xB7
1 0 0x94/0x95
1 1 0xB4/0xB5

Note: Other Parade devices use 96/B6, so only 94/B4 are used for this part.

=T29_WAKE_L:

Desktops use PCIE_WAKE#
Mobiles use S4_WAKE#

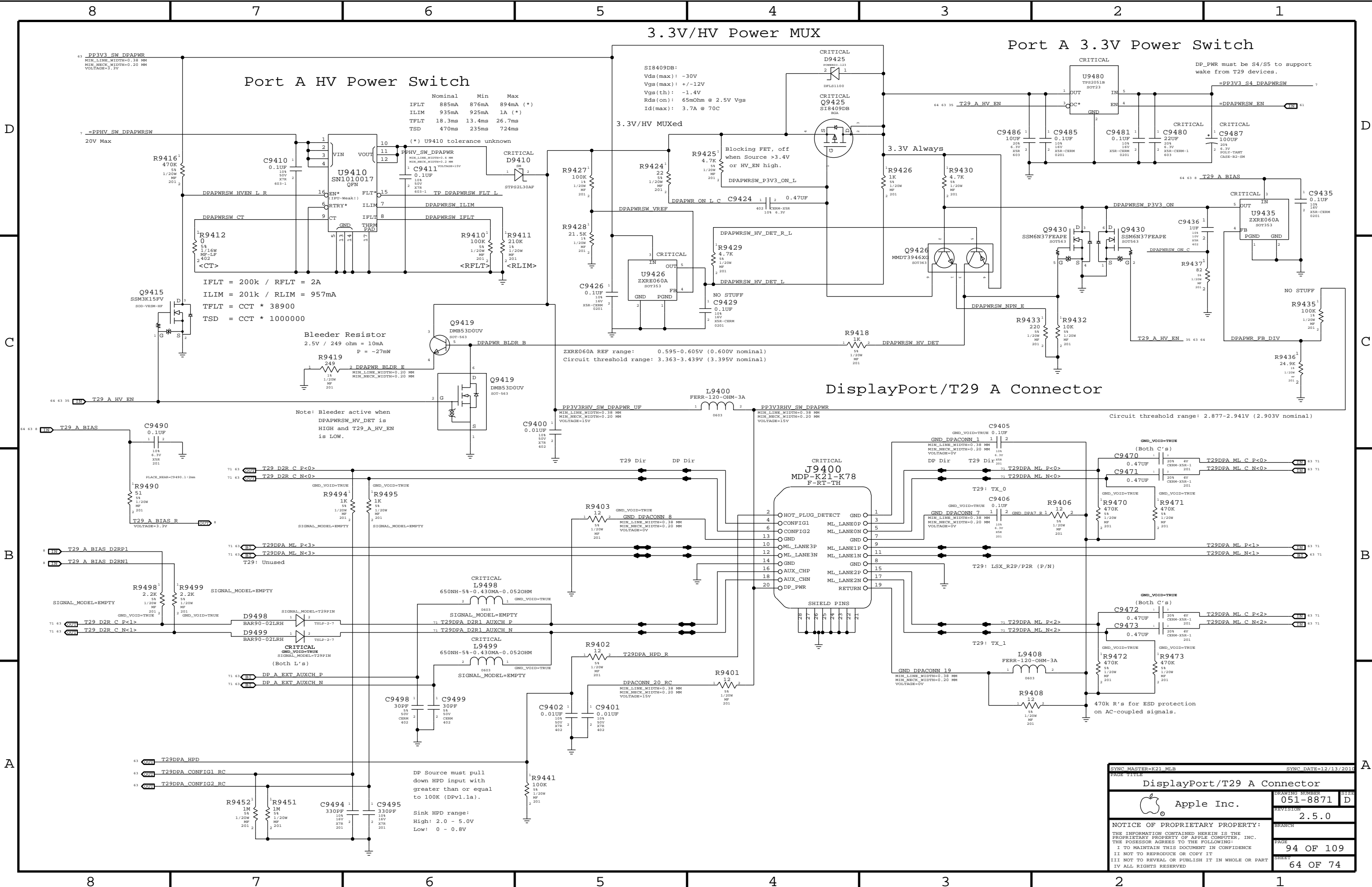
R9330 provides pads for programming/debug of MCU, please make accessible.
If project has space for 10-pin programming header it should be used.

DP/T29 A Low-Speed MUX

Must be 3.3V DP A port power

Note: U9390 ML/HPD defaults to T29 mode so that DP/T29 Display can detect host T29 support using I2C pull-ups on ML<3>. U9390 AUX defaults to DP mode because 100-ohm pull-downs would defeat DP Sink's detection of DP Source.

SYNC MASTER=K21 MLB		SYNC DATE=12/13/2010	
PAGE TITLE		PAGE 11	
DisplayPort/T29 A MUXing		DRAWING NUMBER	051-8871
Apple Inc.		REVISION	2.5.0
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Port A HV Power Switch

	Nominal	Min	Max
IFLT	885mA	876mA	894mA (*)
ILIM	935mA	925mA	1A (*)
TFLT	18.3ms	13.4ms	26.7ms
TSD	470ms	235ms	724ms

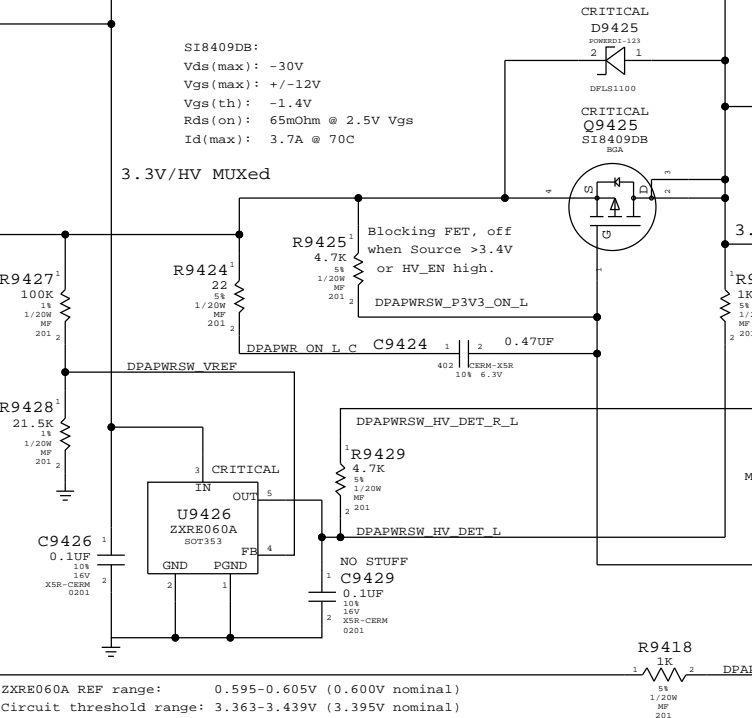
(*) U9410 tolerance unknown

IFLT = 200k / RFLT = 2A
ILIM = 201k / RLIM = 957mA
TFLT = CCT * 38900
TSD = CCT * 1000000

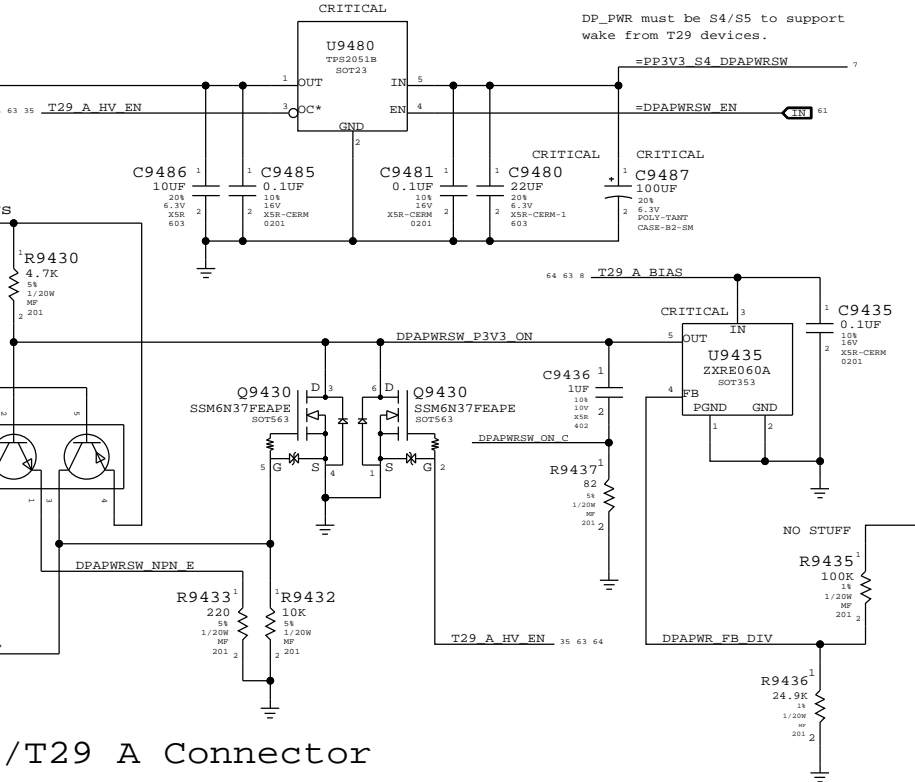
Bleeder Resistor
2.5V / 249 ohm = 10mA
P = ~27mW

Note: Bleeder active when
DPAPWSW_HV_DET is
HIGH and T29_A_HV_EN
is LOW.

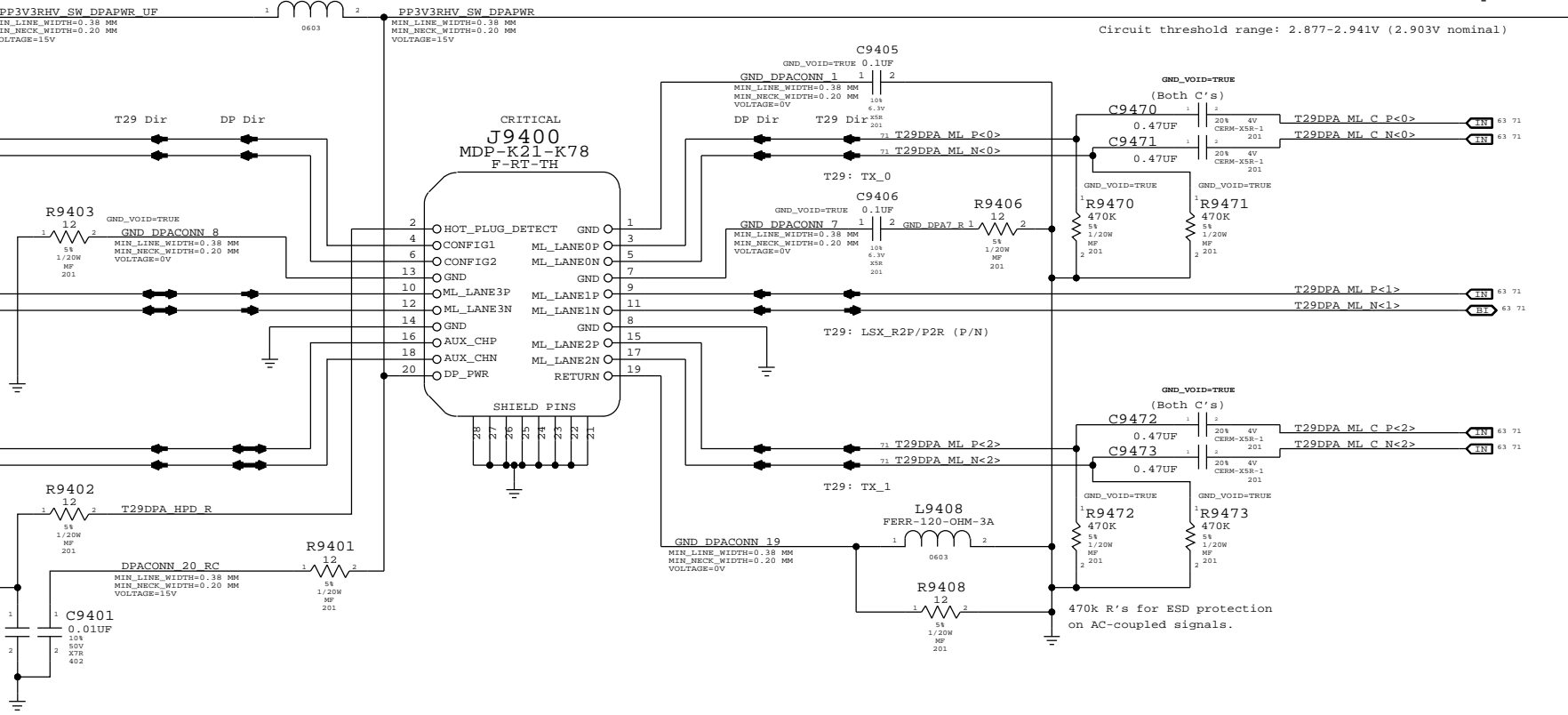
3.3V/HV Power MUX



Port A 3.3V Power Switch



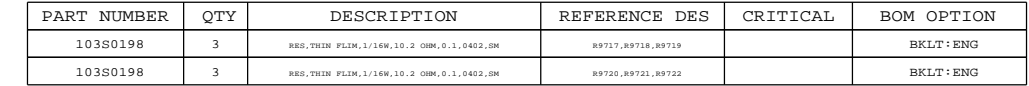
DisplayPort/T29 A Connector




DP Source must pull
down HPD input with
greater than or equal
to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

SYNC MASTER=K21 MLB		SYNC DATE=12/13/2011	
PAGE TITLE			
DisplayPort/T29 A Connector		DRAWING NUMBER	051-8871
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PAGE TITLE			
LCD Backlight Driver			
 Apple Inc.	DRAWING NUMBER		SHEET
	051-8871		D
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CAESAR IV (Ethernet) Constraints							
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_3X	*	=3:1_SPACING	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_CR_DATA	*	8MIL	?












CAESAR IV (Ethernet PHY) Constraints							
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF









SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	8.6 MM	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

FireWire Interface Constraints							
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

Ethernet Net Properties			
ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALI
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALO
	ENET_50S	ENET_3X	ENET_RESET_L
	ENET_MDI	ENET_MDI	ENET_MDI_P<3..0>
	ENET_100D	ENET_MDI	ENET_MDI_N<3..0>
	ENET_50S	ENET_CR_DATA	ENET_CR_DATA<7..0>
	ENET_50S	ENET_CR_DATA	ENET_CR_CMD
	ENET_50S	ENET_CR_DATA	ENET_CR_CLK
	ENET_50S	ENET_CR_DATA	SDCONN_DATA<7..0>
	ENET_50S	ENET_CR_DATA	SDCONN_CMD
	ENET_50S	ENET_CR_DATA	SDCONN_CLK

FireWire Net Properties			
ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
	FW_110D	FW_TP	FW_P0_TPA_P
	FW_110D	FW_TP	FW_P0_TPA_N
	FW_110D	FW_TP	FW_P0_TPB_P
	FW_110D	FW_TP	FW_P0_TPB_N
	FW_110D	FW_TP	FW_P1_TPA_P
	FW_110D	FW_TP	FW_P1_TPA_N
	FW_110D	FW_TP	FW_P1_TPB_P
	FW_110D	FW_TP	FW_P1_TPB_N
Part 2 Not Used			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_I701_55S	*	+1:1_DIFFPAIR	=55_OHM_SR	=55_OHM_SR	=55_OHM_SR	+1:1_DIFFPAIR	+1:1_DIFFPAIR
THERM_I701_55S	*	+1:1_DIFFPAIR	=55_OHM_SR	=55_OHM_SR	=55_OHM_SR	+1:1_DIFFPAIR	+1:1_DIFFPAIR
DIFFPAIR	*	+1:1_DIFFPAIR			+1:1_DIFFPAIR	+1:1_DIFFPAIR	+1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	~2:1_SPACING	?
THERM	*	~2:1_SPACING	?
AUDIO	*	~2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENRT_MDI	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	= STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2046
PCIE	GND	*	GND_P2046
SATA	GND	*	GND_P2046
USB	GND	*	GND_P2046
CLK_PCIE	SR_POWER	*	PWR_P2046
SATA	SR_POWER	*	PWR_P2046
USB	SR_POWER	*	PWR_P2046

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLE	QND	*	QND_P25M
MEM_CMD	QND	*	QND_P25M
MEM_CTRL	QND	*	QND_P25M
MEM_DATA	QND	*	QND_P25M
MEM_DQS	QND	*	QND_P25M

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MKB_400 OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
MKB_720 OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
MKB_370 OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
MKB_850 OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_850 OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.076 MM OVERRIDE	10 MM OVERRIDE	OVERRIDE	OVERRIDE
USB_850 OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	800 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
CLK_PCIE_9D0 OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE

ELECTRICAL_CONSTRAINT_SET		PROVIDES	REQUIRES	PROVIDES	REQUIRES
		ENET_100D	ENETCONN	ENETCONN P<3..0>	
		ENET_100D	ENETCONN	ENETCONN N<3..0>	
		SATA_90D	SATA	SATA ODD D2R UF P	
		SATA_90D	SATA	SATA ODD D2R UF N	
		SATA_90D	SATA	SATA HDD D2R RDRVR OUT P	
		SATA_90D	SATA	SATA HDD D2R RDRVR OUT N	
		SATA_90D	SATA	SATA HDD R2D RDRVR IN P	
		SATA_90D	SATA	SATA HDD R2D RDRVR IN N	
		SATA_90D	SATA	SATA HDD D2R RDRVR IN P	
		SATA_90D	SATA	SATA HDD D2R RDRVR IN N	
		SATA_90D	SATA	SATA HDD R2D RDRVR OUT P	
		SATA_90D	SATA	SATA HDD R2D RDRVR OUT N	
	SENSE_DIFFPAIR	THERM_1T01_55S	THERM	CPUTHMSNS D2 P	
		THERM_1T01_55S	THERM	CPUTHMSNS D2 N	
	CPU_THERMD	THERM_1T01_55S	THERM	CPU_THERMD P	
		THERM_1T01_55S	THERM	CPU_THERMD N	
	SENSE_DIFFPAIR	THERM_1T01_55S	THERM	T29_THERMD P	
		THERM_1T01_55S	THERM	T29_THERMD N	
	SENSE_DIFFPAIR	THERM_1T01_55S	THERM	T29_MLBBOT_THMSNS P	
		THERM_1T01_55S	THERM	T29_MLBBOT_THMSNS N	
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS_HS_COMPUTING N	
		SENSE_1T01_55S	SENSE	ISNS_HS_COMPUTING P	
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS_HS_OTHER N	
		SENSE_1T01_55S	SENSE	ISNS_HS_OTHER P	
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	CPUVCCIOS0_CS N	
		SENSE_1T01_55S	SENSE	CPUVCCIOS0_CS P	
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	CPUIMVP_ISNS1 P	
		SENSE_1T01_55S	SENSE	CPUIMVP_ISNS1 N	
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	CPUIMVP_ISNS2 P	
		SENSE_1T01_55S	SENSE	CPUIMVP_ISNS2 N	
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	CPUIMVP_ISNS1G P	
		SENSE_1T01_55S	SENSE	CPUIMVP_ISNS1G N	
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	CPUIMVP_ISUM_R P	
		SENSE_1T01_55S	SENSE	CPUIMVP_ISUM_R N	
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	CPUIMVP_ISUMG_R P	
		SENSE_1T01_55S	SENSE	CPUIMVP_ISUMG_R N	
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	CPUIMVP_ISNS P	
		SENSE_1T01_55S	SENSE	CPUIMVP_ISNS N	
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	VCCSA0_CS P	
		SENSE_1T01_55S	SENSE	VCCSA0_CS N	
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	CPUIMVP_ISUMG P	
		SENSE_1T01_55S	SENSE	CPUIMVP_ISUMG N	
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS_CPU N	
		SENSE_1T01_55S	SENSE	ISNS_CPU P	
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS_HDD N	
		SENSE_1T01_55S	SENSE	ISNS_HDD P	
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS_HDD_R N	
		SENSE_1T01_55S	SENSE	ISNS_HDD_R P	
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS_LCDBKLT N	
		SENSE_1T01_55S	SENSE	ISNS_LCDBKLT P	
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS_ODD N	
		SENSE_1T01_55S	SENSE	ISNS_ODD P	
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS_ODD_R N	
		SENSE_1T01_55S	SENSE	ISNS_ODD_R P	
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS_1V5_S3 N	
		SENSE_1T01_55S	SENSE	ISNS_1V5_S3 P	
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS_P1V8GPU_R N	
		SENSE_1T01_55S	SENSE	ISNS_P1V8GPU_R P	
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS_AIRPORT N	
		SENSE_1T01_55S	SENSE	ISNS_AIRPORT P	
	LVDS_90D	LVDS	LVDS	LVDS_CONN_A_CLK_F N	
	LVDS_90D	LVDS	LVDS	LVDS_CONN_A_CLK_F P	

Audio Net Properties

		NET_TYPE		
ELECTRICAL_CONSTRAINT_SET		PHYSICAL	SPACING	
NAME	SPKRAMP_INR	DIEFFPAIR	AUDIO	SPKRAMP_INR_P 6 39 50 73
NAME		DIEFFPAIR	AUDIO	SPKRAMP_INR_N 6 39 50 73
NAME	MAX98300_R	DIEFFPAIR	AUDIO	MAX98300_R_P 60
NAME		DIEFFPAIR	AUDIO	MAX98300_R_N 60

ELECTRICAL_CONSTRAINT_SET		NET_TYPE	
	PORTNAME	APPLICABLE	
	PCIE_CLK100M_AP	CLK_PCIE_90D	PCIE_CLK100M_AP_CONN_P
		CLK_PCIE_90D	PCIE_CLK100M_AP_CONN_N
	1T01_DIEFFPAIR		CHGR_CSI_R_P
	1T01_DIEFFPAIR		CHGR_CSI_R_N
	1T01_DIEFFPAIR		CHGR_CSO_R_P
	1T01_DIEFFPAIR		CHGR_CSO_R_N
USB_EPCA	USB_85D	USB	USB2_EXTM_MUXED_P
USB_EPCA	USB_85D	USB	USB2_EXTM_MUXED_N
USB_EPCA	USB_85D	USB	USB2_LT1_P
USB_EPCA	USB_85D	USB	USB2_LT1_N
	USB_85D	USB	CONN_USB2_BT_P
	USB_85D	USB	CONN_USB2_BT_N
	USB_85D	USB	USB_LT2_P
	USB_85D	USB	USB_LT2_N
	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_C_P
	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_C_N
SPK_OUT	DIEFFPAIR	AUDIO	SPKRAMP_L_P_OUT
SPK_OUT	DIEFFPAIR	AUDIO	SPKRAMP_L_N_OUT
SPK_OUT	DIEFFPAIR	AUDIO	SPKRAMP_SUB_P_OUT
SPK_OUT	DIEFFPAIR	AUDIO	SPKRAMP_SUB_N_OUT
SPK_OUT	DIEFFPAIR	AUDIO	SPKRAMP_R_P_OUT
SPK_OUT	DIEFFPAIR	AUDIO	SPKRAMP_R_N_OUT
AUD_DIFF	1T01_DIEFFPAIR	AUDIO	SSM2315_SUB_N
AUD_DIFF	1T01_DIEFFPAIR	AUDIO	SSM2315_SUB_P
AUD_DIFF	1T01_DIEFFPAIR	AUDIO	SSM2315_L_N
AUD_DIFF	1T01_DIEFFPAIR	AUDIO	SSM2315_L_P
AUD_DIFF	1T01_DIEFFPAIR	AUDIO	SSM2315_R_N
AUD_DIFF	1T01_DIEFFPAIR	AUDIO	SSM2315_R_P
AUD_DIFF	1T01_DIEFFPAIR	AUDIO	AUD_LO2_N_R
AUD_DIFF	1T01_DIEFFPAIR	AUDIO	AUD_LO2_P_R
AUD_DIFF	1T01_DIEFFPAIR	AUDIO	AUD_LO1_N_R
AUD_DIFF	1T01_DIEFFPAIR	AUDIO	AUD_LO1_P_R
AUD_DIFF	1T01_DIEFFPAIR	AUDIO	AUD_LO2_N_L
AUD_DIFF	1T01_DIEFFPAIR	AUDIO	AUD_LO2_P_L
AUD_DIFF	1T01_DIEFFPAIR	AUDIO	SPKRAMP_INL_P
AUD_DIFF	1T01_DIEFFPAIR	AUDIO	SPKRAMP_INL_N
SPKRAMP_INR	DIEFFPAIR	AUDIO	SPKRAMP_INR_P
AUD_DIFF	DIEFFPAIR	AUDIO	SPKRAMP_INR_N
AUD_DIFF	1T01_DIEFFPAIR	AUDIO	SPKRAMP_INSUB_P
AUD_DIFF	1T01_DIEFFPAIR	AUDIO	SPKRAMP_INSUB_N
	USB_85D	USB	USB_TPAD_R_P
	USB_85D	USB	USB_TPAD_R_N
		SB_POWER	PP3V3_S5
		SB_POWER	PP3V3_S0
		GND	GND


Misc Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
PHYS	(USB_EXTN)	USB_85D	USB	USB EXTN MUXED P
PHYS	(USB_EXTN)	USB_85D	USB	USB EXTN MUXED N
PHYS	(USB_EXTN)	USB_85D	USB	USB LTI P
PHYS	(USB_EXTN)	USB_85D	USB	USB LTI N
PHYS	(USB_TPAD)	USB_85D	USB	USB TPAD CONN P
PHYS	(USB_TPAD)	USB_85D	USB	USB TPAD CONN N
PHYS	SMBUS_SMC_MGMT_SDA	SMB_55S	SMB	I2C SMC SMS SDA R
PHYS	SMBUS_SMC_MGMT_SCL	SMB_55S	SMB	I2C SMC SMS SCL R
PHYS		SMB_55S	SMB	I2C TCON SCL
PHYS		SMB_55S	SMB	I2C TCON SDA
PHYS		SMB_55S	SMB	I2C TCON SCL CONN
PHYS		SMB_55S	SMB	I2C TCON SDA CONN


Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

BASIC MASTER CONSTRAINTS		BASIC DATE=04/08/2011	
PAGE TITLE			
Project Specific Constraints			
 Apple Inc.		DRAWING NUMBER	051-8871
		SIZE	D
		REVISION	2.5.0
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8		7		6		5		4		3		2		1		
K90i Board-Specific Spacing & Physical Constraints																
BOARD LAYERS				BOARD AREAS				BOARD UNITS (MIL or MM)		ALLEGRO VERSION						
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM				NO_TYPE, BGA				MM		15.5.1						
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP									
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM									
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT									
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP									
50_OHM_SE	TOP, BOTTOM	Y	0.110 MM	0.090 MM												
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD									
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP									
40_OHM_SE	TOP, BOTTOM	Y	0.170 MM	0.170 MM												
40_OHM_SE	ISL3, ISL4, ISL9, ISL10	Y	0.140 MM	0.140 MM	=STANDARD	=STANDARD	=STANDARD									
40_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD									
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP									
37_OHM_SE	TOP, BOTTOM	Y	0.195 MM	0.1 MM												
37_OHM_SE	ISL3, ISL4, ISL9, ISL10	Y	0.160 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD									
37_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD									
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP									
27P4_OHM_SE	TOP, BOTTOM	Y	0.310 MM	0.2 MM												
27P4_OHM_SE	*	Y	0.250 MM	0.2 MM	=STANDARD	=STANDARD	=STANDARD									
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP									
55_OHM_SE	TOP, BOTTOM	Y	0.090 MM	0.090 MM												
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD									
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP									
72_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD									
72_OHM_DIFF	ISL3, ISL10	Y	0.135 MM	0.135 MM		0.130 MM	0.130 MM									
72_OHM_DIFF	ISL4, ISL9	Y	0.155MM	0.155 MM		0.130 MM	0.130 MM									
72_OHM_DIFF	TOP, BOTTOM	Y	0.165 MM	0.165 MM		0.130 MM	0.130 MM									
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP									
85_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD									
85_OHM_DIFF	ISL3, ISL10	Y	0.095 MM	0.1 MM		0.170 MM	0.170 MM									
85_OHM_DIFF	ISL4, ISL9	Y	0.115 MM	0.115 MM		0.170 MM	0.170 MM									
85_OHM_DIFF	TOP, BOTTOM	Y	0.130 MM	0.130 MM		0.195 MM	0.195 MM									
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP									
90_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD									
90_OHM_DIFF	ISL3, ISL10	Y	0.089 MM	0.089 MM		0.210 MM	0.210 MM									
90_OHM_DIFF	ISL4, ISL9	Y	0.105 MM	0.105 MM		0.210 MM	0.210 MM									
90_OHM_DIFF	TOP, BOTTOM	Y	0.115 MM	0.115 MM		0.210 MM	0.210 MM									
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP									
100_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD									
100_OHM_DIFF	ISL3, ISL10	Y	0.074 MM	0.074 MM		0.250 MM	0.250 MM									
100_OHM_DIFF	ISL4, ISL9	Y	0.085 MM	0.085 MM		0.250 MM	0.250 MM									
100_OHM_DIFF	TOP, BOTTOM	Y	0.091 MM	0.091 MM		0.200 MM	0.200 MM									
NOTE: 110_DIFF is 110-ohms differential impedance on outer layers and 105-ohms on inner layers.																
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP									
110_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD									
110_OHM_DIFF	ISL3, ISL10	N	0.070 MM	0.070 MM		0.330 MM	0.330 MM									
110_OHM_DIFF	ISL4, ISL9	Y	0.071 MM	0.071 MM		0.300 MM	0.300 MM									
110_OHM_DIFF	TOP, BOTTOM	Y	0.077 MM	0.077 MM		0.280 MM	0.280 MM									
NOTE: These are Intel recommended impedances for PEG, unused on K90i.																
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP									
48_OHM_SE	TOP, BOTTOM	Y	0.120 MM	0.165 MM												
48_OHM_SE	*	Y	0.097 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD									
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP									
80_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD									
80_OHM_DIFF	ISL3, ISL10	Y	0.110 MM	0.110 MM		0.170 MM	0.170 MM									
80_OHM_DIFF	ISL4, ISL9	Y	0.129 MM	0.129 MM		0.170 MM	0.170 MM									
80_OHM_DIFF	TOP, BOTTOM	Y	0.145 MM	0.145 MM		0.180 MM	0.180 MM									
SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING		WEIGHT				NET_SPACING_TYPE1		NET_SPACING_TYPE2		AREA_TYPE		SPACING_RULE_SET	
DEFAULT		*	0.1 MM		?				*		*		BGA		BGA_P1MM	
STANDARD		*	=DEFAULT		?				MEM_CLK		*		BGA		BGA_P2MM	
BGA_P1MM		*	=DEFAULT		?				CLK_PCIE		*		BGA		BGA_P2MM	
BGA_P2MM		*	=DEFAULT		?				CLK_SLOW		*		BGA		BGA_P2MM	
SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING		WEIGHT				SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING		WEIGHT		
1.5:1_SPACING		*	0.15 MM		?				2X_DIELECTRIC		*		0.140 MM		?	
2:1_SPACING		*	0.2 MM		?				3X_DIELECTRIC		*		0.210 MM		?	
2.5:1_SPACING		*	0.25 MM		?				4X_DIELECTRIC		*		0.280 MM		?	
3:1_SPACING		*	0.3 MM		?				5X_DIELECTRIC		*		0.350 MM		?	
4:1_SPACING		*	0.4 MM		?				7X_DIELECTRIC		*		0.490 MM		?	
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP								
1:1_DIFFPAIR		*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM							
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP								
85_DIFF_BGA		*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF							
85_DIFF_BGA		ISL3, ISL4	Y	0.075 MM	0.075 MM			0.125 MM	0.125 MM							
85_DIFF_BGA		ISL9, ISL10	Y	0.075 MM	0.075 MM			0.125 MM	0.125 MM							
NOTE: 85_DIFF_BGA is 85-ohms differential impedance on outer layers and 80-ohms on inner layers.																
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP								
90_DIFF_BGA		*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF							
90_DIFF_BGA		ISL3, ISL4	Y	0.075 MM	0.075 MM			0.125 MM	0.125 MM							
90_DIFF_BGA		ISL9, ISL10	Y	0.075 MM	0.075 MM			0.125 MM	0.125 MM							
NOTE: 90_DIFF_BGA is 90-ohms differential impedance on outer layers and 85-ohms on inner layers.																
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP								
100_DIFF_BGA		*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF							
100_DIFF_BGA		ISL3, ISL4	Y	0.075 MM	0.075 MM			0.125 MM	0.125 MM							
100_DIFF_BGA		ISL9, ISL10	Y	0.075 MM	0.075 MM			0.125 MM	0.125 MM							
NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.																
SYNCH MASTER CONSTRAINTS																

PCB Rule Definitions															
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